MT6799 LTE-A Smartphone Appliciation Processor Technical Brief

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1 System Overview

The MT6799 hardware family is a highly integrated baseband platform incorporating both modem and application processing subsystems. The chip integrates ARM® Artemis operating up to 2.6GHz, ARM® Cortex-A53 operating up to 2.2GHz, ARM® Cortex-A35 operating up to 1.9GHz, an MIPS@interAptiv MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and UFS/eMMC/SD cards.

The application processor, a Tri-cluster having Multi-core ARM® Artemis, ARM® Cortex-A53 MPCore™, and ARM® Cortex-A35 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.

All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

An MIPS® interAptiv, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 7/10, Category 29 HSDPA downlink and Category 8 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6799

- Dual-core ARM® Artemis MPCore™ operating up to 2.6GHz
- Quad-core ARM® Cortex-A53 MPCore™ operating at 2.2GHz
- Quad-core ARM® Cortex-A35 MPCore™ operating at 1.9GHz
- LPDDR4/4x up to 8GB, 1600MHz
- LTE Cat 7/10 (300/450Mps)
- Resolution up to WQXGA
- IMG® 7XTP-MT x4 3D Graphics
- OpenGL ES 3.1 3D graphic accelerator
- ISP supports 28MP@30fps, 14 bits
- Flexible and reconfigurable image processing unit to exploit ISP
- HEVC 8/10 bits 4K2K@30fps decoder
- VP9 4K2K@30fps encoder
- Headphone ANC/handset ANC
- Dedicated audio DSP (Cortex-M4)

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - Supports eMMC/UFS boot
  - Supports LPDDR4/4x

- **AP MCU subsystem**
  - Dual-core ARM® 2.6Ghz Artemis MPCoreTM with 64KB L1 I-cache, 64KB L1 D-cache and 1MB unified L2 cache
  - Quad-core ARM® 2.2Ghz Cortex-A53 MPCoreTM with 32KB L1 I-cache, 32KB L1 D-cache and 512KB unified L2 cache
  - Quad-core ARM® 1.9Ghz Cortex-A35 MPCoreTM with 32KB L1 I-cache, 32KB L1 D-cache and 512KB unified L2 cache
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - DVFS technology with adaptive operating voltage from 0.55V to 1.0V

- **MD MCU subsystem**
  - MIPS® interAptiv processors with max. 900 MHz operation frequency
  - 64KB I-cache, 32KB D-cache
  - 384/128KB I-D/TCM (tightly-coupled memory)
  - 512KB unified L2 cache
  - Coresonic DSP for running LTE modem tasks
  - FD216 DSP for running modem/voice tasks, with max. 312MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security
  - UFS in-line encryption and full-disk encryption engine
  - ARM ® CryptoCell

- **External memory interface**
  - LPDDR4/4x up to 8GB
  - Four channel with 16-bit data bus width
  - Memory clock up to 1600MHz
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - Supports USB3.0 SS
  - USB2.0 host mode
  - IC-USB device mode
  - eMMC5.1
  - UFS2.1
  - 4 UART for debugging and applications
  - 10 SPI master for external device
  - 8 I2C/I3C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 1 set of memory card controllers supporting SD/SDHC/SDIO3.0+ protocols

- **Operating conditions**

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- Core voltage: 0.65V
- I/O voltage: 1.2V/1.8V/2.8V/3.3V
- Memory: 0.6V/1.1V
- LCM interface: 1.8V
- Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: MLPoP
  - 14.0mm*14.0mm
  - Height: 0.67mm maximum w/o memory
  - BTM ball count: 930 balls
  - TOP ball count: 376 balls
  - BTM ball pitch: 0.4mm
  - TOP ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 450Mbps downlink, 100Mbps uplink
  - Carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to Downlink 3 CCs/Uplink 2 CCs
  - 4-port CRS/2-port DMRS 2-layer SU-MIMO with 8-port CSIRS based CSI reporting per CC
  - MU-MIMO supporting 2-layer joint detection per CC
  - Supports feICIC
  - Supports MBMS
  - Supports LAA
  - Supports LWA

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 11-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology

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- VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports max. 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Supports Simultaneous Hybrid Dual Receiver (SHDR)
  - Supports 1x Diversity
  - Supports SRLTE

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1.4 Multimedia Features

- **Display**
  - Portrait panel resolution up to WQXGA (2,560*1,600) 120fps
  - MIPI DSI interface (8 data lanes)
  - MiraVisionTM for picture quality enhancement
  - ClearMotionTM for DTV-class video quality
  - Embedded LCD gamma correction
  - True colors
  - 12 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Memory color adjustment
  - Adaptive contrast enhancement
  - Content aware local tone enhancement
  - Image/video/graphic sharpness enhancement
  - SmartScreen™: Dynamic backlight scaling and sunlight visibility
  - Smoothing brightness control for LCD and AMOLED
  - Quality-Preserving Power Saving (QPPS) engine for LCD and AMLED
  - Ultra dimming
  - BluLight defender
  - Chameleon display
  - Wide gamut and color correction
  - VESA display stream compression

- **Graphics**
  - IMG® 7XTP-MT x4 3D Graphics
  - OpenGL ES 3.1 3D graphic accelerator capable of processing 425M tri/sec and 6,800M pixel/sec@850MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Integrated image signal processor supports 28MP@30fps, 14 bits
  - Flexible and reconfigurable image processing unit to exploit ISP
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Video with shallow depth of field
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 28M sensors)
  - 3 MIPI CSI-2 high-speed camera serial interfaces; all are 4 data lane
  - PIP (picture in picture), [13MP + 13MP]@30fps
  - Hardware JPEG encoder: Baseline encoding with 200M pixel/sec. Continuous shot with 28M pixel@ 7fps
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC 8/10-bit decoder 2160p@30fps
  - VP9 8/10-bit decoder 2160p@30fps
  - H.264 8/10-bit decoder: 2160p@30fps
  - Sorenson H.263/H.263 decoder: 1080p @ 60fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p@60fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p@60fps/40Mbps

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- VC1 decoder: 1080p@60fps/40Mbps
- VP8 decoder: 1080p@60fps/40Mbps
- MPEG2 decoder: 1080p@60fps/40Mbps
- MPEG1 decoder: 1080p@60fps/40Mbps
- MPEG-4 encoder: Simple profile D1@30fps
- H.263 encoder: Simple profile D1@30fps
- H.264 encoder: High profile 1080p@60fps
- HEVC encoder: Main profile 2160p@30fps
- VP9 encoder: 2160p@30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 384kHz
  - Audio content sample formats supported: 16-bit/24-bit/32-bit, mono/stereo
  - Interfaces supported: I2S, PCM, TDM, SoundWire
  - External CODEC I2S interface supports 16-bit/24-bit/32-bit, mono/stereo, up to 384kHz
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness (MB-DRC), BesSurround, Android built-in post processing
  - Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM
  - Voice wakeup
  - Headphone ANC/handset ANC
  - Dedicated audio DSP (Cortex-M4)

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Compensation filter and digital gain for both uplink and downlink paths
  - MagiNRdual (Dual-MIC noise cancellation)
  - MagiNR (noise suppression)
  - MagiAEC (echo cancellation & echo suppression)
  - MagiConference (echo cancellation and Dual-MIC second source cancellation for speaker phone)
  - MagiLoudness (maximizes loudness while controlling the max. receiver output power; feed-forward receiver protection)
  - MagiClarity (enhances voice clarity based on near-end environment noise)
  - MagiTDNC (removes TDD noise at GSM Link)
  - Dual-MIC stereo sound recording w/o wind noise rejection
  - Dual-MIC voice tracking
  - Voice wakeup
  - Headphone ANC/handset ANC
  - Dedicated audio DSP (Cortex-M4)

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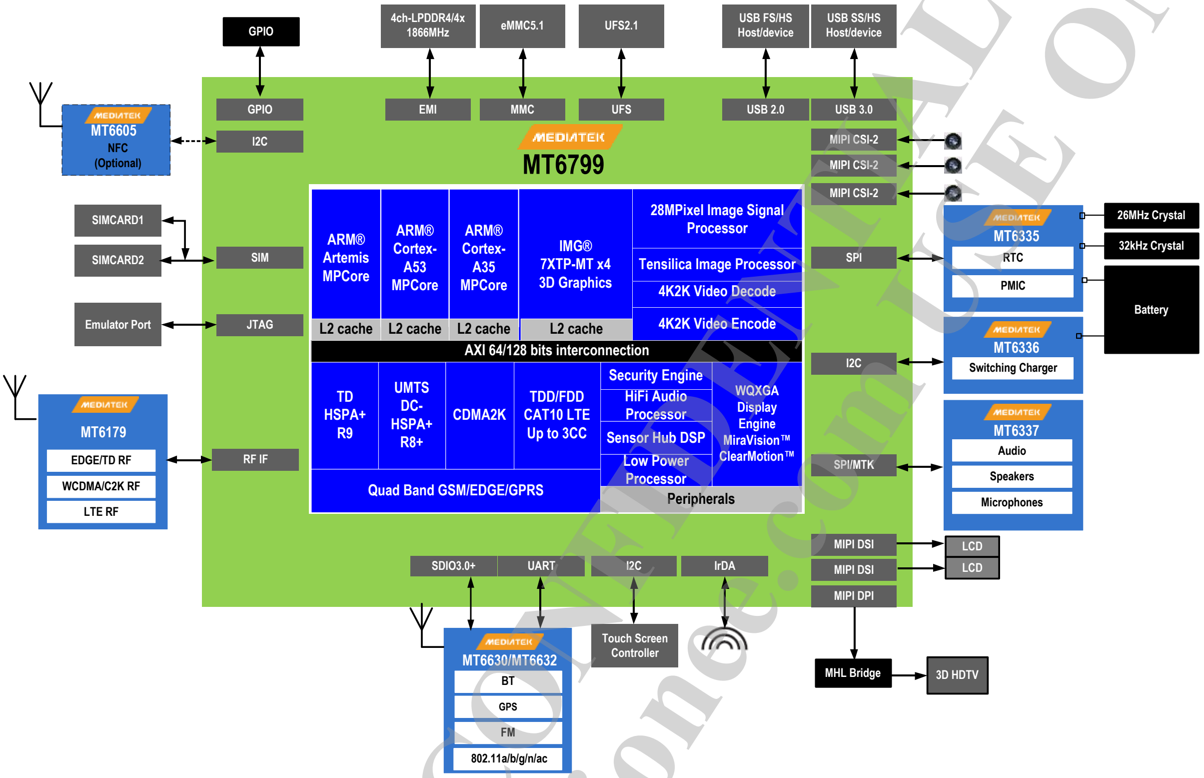

Figure 1-1. MT6799 block diagram

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

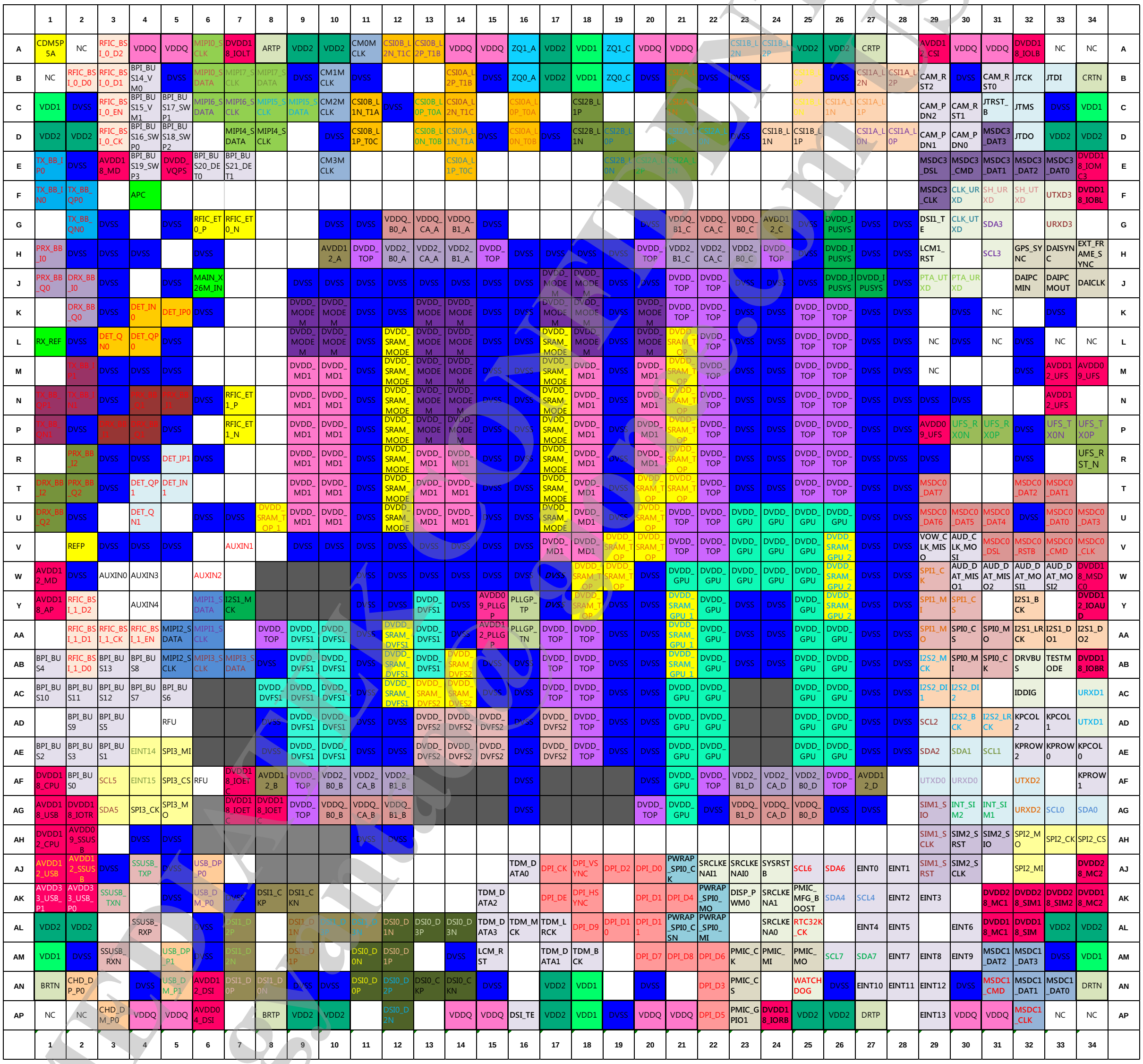

Figure 2-1. Bottom ball map view of MT6799

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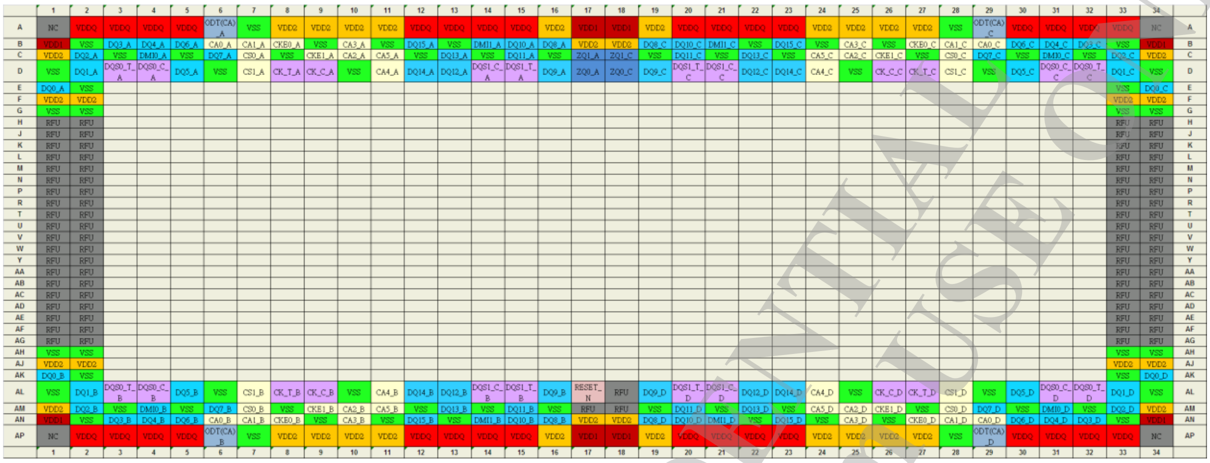

Figure 2-2. Top ball map view of MT6799

2.1.2 Pin Coordinate

Table 2-1. Bottom pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	CDM5P5A	AL24	SRCLKENA0	K23	DVSS
A10	VDD2	AL25	RTC32K_CK	K24	DVSS
A11	CM0MCLK	AL27	EINT4	K25	DVDD_TOP
A12	CSI0B_L2N_T1C	AL28	EINT5	K26	DVDD_TOP
A13	CSI0B_L2P_T1B	AL30	EINT6	K27	DVSS
A14	VDDQ	AL31	DVDD18_MC1	K28	DVSS
A15	VDDQ	AL32	DVDD18_SIM	K3	DVSS
A16	ZQ1_A	AL33	VDD2	K30	DVSS
A17	VDD2	AL34	VDD2	K31	NC
A18	VDD1	AL4	SSUSB_RXP	K33	DVSS
A19	ZQ1_C	AL6	DVSS	K4	DET_IN0
A2	NC	AL7	DSI1_D2P	K5	DET_IP0
A20	VDDQ	AL9	DSI1_D1N	K6	DVSS
A21	VDDQ	AM1	VDD1	K9	DVDD_MODEM
A23	CSI1B_L2N	AM11	DSI0_D0N	L1	RX_REF
A24	CSI1B_L2P	AM12	DSI0_D1P	L10	DVDD_MODEM
A25	VDD2	AM14	DVSS	L11	DVSS
A26	VDD2	AM15	LCM_RST	L12	DVDD_SRAM_MODEM
A27	CRTP	AM17	TDM_DATA1	L13	DVDD_MODEM
A29	AVDD12_CSI	AM18	TDM_BCK	L14	DVDD_MODEM
A3	RFIC_BSI_0_D2	AM2	DVSS	L15	DVSS
A30	VDDQ	AM20	DPI_D7	L16	DVSS
A31	VDDQ	AM21	DPI_D8	L17	DVDD_SRAM_MODEM
A32	DVDD18_IOLB	AM22	DPI_D6	L18	DVDD_MODEM
A33	NC	AM23	PMIC_CK	L19	DVSS
A34	NC	AM24	PMIC_MI	L2	DVSS
A4	VDDQ	AM25	PMIC_MO	L20	DVDD_MODEM
A5	VDDQ	AM26	SCL7	L21	DVDD_SRAM_TOP

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A6	MIPI0_SCLK	AM27	SDA7	L22	DVDD_TOP
A7	DVDD18_IOLT	AM28	EINT7	L23	DVSS
A8	ARTP	AM29	EINT8	L24	DVSS
A9	VDD2	AM3	SSUSB_RXN	L25	DVDD_TOP
AA10	DVDD_DVFS1	AM30	EINT9	L26	DVDD_TOP
AA11	DVSS	AM31	MSDC1_DAT2	L27	DVSS
AA12	DVDD_SRAM_DVFS1	AM32	MSDC1_DAT3	L28	DVSS
AA13	DVDD_DVFS1	AM33	DVSS	L29	NC
AA14	DVSS	AM34	VDD1	L3	DET_QN0
AA15	AVDD12_PLLGP	AM5	USB_DP_P1	L30	DVSS
AA16	PLLGP_TN	AM6	DVSS	L31	NC
AA17	DVDD_TOP	AM7	DSI1_D2N	L32	DVSS
AA18	DVDD_TOP	AM9	DSI1_D1P	L33	NC
AA19	DVSS	AN1	BRTN	L34	NC
AA2	RFIC_BSI_1_D1	AN10	DVSS	L4	DET_QP0
AA20	DVSS	AN11	DSI0_D0P	L5	DVSS
AA21	DVDD_SRAM_GPU_1	AN12	DSI0_D2P	L9	DVDD_MODEM
AA22	DVDD_GPU	AN13	DSI0_CKP	M10	DVDD_MD1
AA23	DVSS	AN14	DSI0_CKN	M11	DVSS
AA24	DVSS	AN15	DVSS	M12	DVDD_SRAM_MODEM
AA25	DVDD_GPU	AN17	VDD2	M13	DVDD_MODEM
AA26	DVDD_GPU	AN18	VDD1	M14	DVDD_MODEM
AA27	DVSS	AN2	CHD_DP_P0	M15	DVSS
AA28	DVSS	AN20	DVSS	M16	DVSS
AA29	SPI1_MO	AN22	DPI_D3	M17	DVDD_SRAM_MODEM
AA3	RFIC_BSI_1_CK	AN23	PMIC_CS	M18	DVDD_MD1
AA30	SPI0_CS	AN25	WATCHDOG	M19	DVSS
AA31	SPI0_MO	AN26	DVSS	M2	TX_BB_IP1
AA32	I2S1_LRCK	AN27	EINT10	M20	DVDD_MD1
AA33	I2S1_DO1	AN28	EINT11	M21	DVDD_SRAM_TOP
AA34	I2S1_DO2	AN29	EINT12	M22	DVDD_TOP
AA4	RFIC_BSI_1_EN	AN30	DVSS	M23	DVSS
AA5	MIPI2_SDATA	AN31	MSDC1_CMD	M24	DVSS
AA6	MIPI1_SCLK	AN32	MSDC1_DAT1	M25	DVDD_TOP
AA8	DVDD_TOP	AN33	MSDC1_DAT0	M26	DVDD_TOP
AA9	DVDD_DVFS1	AN34	DRTN	M27	DVSS
AB1	BPI_BUS4	AN4	DVSS	M28	DVSS
AB10	DVDD_DVFS1	AN5	USB_DM_P1	M29	NC
AB11	DVSS	AN6	AVDD12_DSI	M3	DVSS
AB12	DVDD_SRAM_DVFS1	AN7	DSI1_D0P	M32	DVSS
AB13	DVDD_DVFS1	AN8	DSI1_D0N	M33	AVDD12_UFS
AB14	DVDD_SRAM_DVFS2	AN9	DVSS	M34	AVDD09_UFS
AB15	DVSS	AP1	NC	M4	DVSS
AB16	DVSS	AP10	VDD2	M5	DVSS
AB17	DVDD_TOP	AP12	DSI0_D2N	M9	DVDD_MD1
AB18	DVDD_TOP	AP14	VDDQ	N1	TX_BB_QP1
AB19	DVSS	AP15	VDDQ	N10	DVDD_MD1
AB2	RFIC_BSI_1_D0	AP16	DSI_TE	N11	DVSS
AB20	DVSS	AP17	VDD2	N12	DVDD_SRAM_MODEM
AB21	DVDD_SRAM_GPU_1	AP18	VDD1	N13	DVDD_MODEM

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AB22	DVDD_GPU	AP19	DVSS	N14	DVDD_MODEM
AB23	DVSS	AP2	NC	N15	DVSS
AB24	DVSS	AP20	VDDQ	N16	DVSS
AB25	DVDD_GPU	AP21	VDDQ	N17	DVDD_SRAM_MODEM
AB26	DVDD_GPU	AP22	DPI_D5	N18	DVDD_MD1
AB27	DVSS	AP23	PMIC_GPIO1	N19	DVSS
AB28	DVSS	AP24	DVDD18_IORB	N2	TX_BB_IN1
AB29	I2S2_MCK	AP25	VDD2	N20	DVDD_MD1
AB3	BPI_BUS13	AP26	VDD2	N21	DVDD_SRAM_TOP
AB30	SPI0_MI	AP27	DRTP	N22	DVDD_TOP
AB31	SPI0_CK	AP29	EINT13	N23	DVSS
AB32	DRVBUS	AP3	CHD_DM_P0	N24	DVSS
AB33	TESTMODE	AP30	VDDQ	N25	DVDD_TOP
AB34	DVDD18_IOBR	AP31	VDDQ	N26	DVDD_TOP
AB4	BPI_BUS8	AP32	MSDC1_CLK	N27	DVSS
AB5	MIPI2_SCLK	AP33	NC	N28	DVSS
AB6	MIPI3_SCLK	AP34	NC	N29	DVSS
AB7	MIPI3_SDATA	AP4	VDDQ	N3	DVSS
AB8	DVSS	AP5	VDDQ	N30	DVSS
AB9	DVDD_DVFS1	AP6	AVDD04_DSI	N33	AVDD12_UFS
AC1	BPI_BUS10	AP8	BRTP	N4	PRX_BB_Q1
AC10	DVDD_DVFS1	AP9	VDD2	N5	PRX_BB_I1
AC11	DVSS	B1	NC	N6	DVSS
AC12	DVDD_SRAM_DVFS1	B10	CM1MCLK	N7	RFIC_ET1_P
AC13	DVDD_SRAM_DVFS2	B11	DVSS	N9	DVDD_MD1
AC14	DVDD_SRAM_DVFS2	B14	CSI0A_L2P_T1B	P1	TX_BB_QN1
AC15	DVSS	B15	DVSS	P10	DVDD_MD1
AC16	DVSS	B16	ZQ0_A	P11	DVSS
AC17	DVDD_TOP	B17	VDD2	P12	DVDD_SRAM_MODEM
AC18	DVDD_TOP	B18	VDD1	P13	DVDD_MODEM
AC19	DVSS	B19	ZQ0_C	P14	DVDD_MODEM
AC2	BPI_BUS11	B2	RFIC_BSI_0_D0	P15	DVSS
AC20	DVSS	B20	DVSS	P16	DVSS
AC21	DVDD_GPU	B21	CSI2A_L1P	P17	DVDD_SRAM_MODEM
AC22	DVDD_GPU	B22	DVSS	P18	DVDD_MD1
AC25	DVDD_GPU	B23	DVSS	P19	DVSS
AC26	DVDD_GPU	B25	CSI1B_L0P	P2	DVSS
AC27	DVSS	B26	DVSS	P20	DVDD_MD1
AC28	DVSS	B27	CSI1A_L2N	P21	DVDD_SRAM_TOP
AC29	I2S2_DI1	B28	CSI1A_L2P	P22	DVDD_TOP
AC3	BPI_BUS12	B29	CAM_RST2	P23	DVSS
AC30	I2S2_DI2	B3	RFIC_BSI_0_D1	P24	DVSS
AC32	IDDIG	B30	DVSS	P25	DVDD_TOP
AC34	URXD1	B31	CAM_RST0	P26	DVDD_TOP
AC4	BPI_BUS7	B32	JTCK	P27	DVSS
AC5	BPI_BUS6	B33	JTDI	P28	DVSS
AC8	DVDD_DVFS1	B34	CRTN	P29	AVDD09_UFS
AC9	DVDD_DVFS1	B4	BPI_BUS14_VM0	P3	DRX_BB_I1
AD10	DVDD_DVFS1	B5	DVSS	P30	UFS_RX0N
AD11	DVSS	B6	MIPI0_SDATA	P31	UFS_RX0P

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AD12	DVSS	B7	MIPI7_SCLK	P32	DVSS
AD13	DVDD_DVFS2	B8	MIPI7_SDATA	P33	UFS_TX0N
AD14	DVDD_DVFS2	B9	DVSS	P34	UFS_TX0P
AD15	DVDD_DVFS2	C1	VDD1	P4	DRX_BB_Q1
AD16	DVSS	C10	CM2MCLK	P5	DVSS
AD17	DVDD_DVFS2	C11	CSI0B_L1N_T1A	P7	RFIC_ET1_N
AD18	DVDD_TOP	C12	DVSS	P9	DVDD_MD1
AD19	DVSS	C13	CSI0B_L0P_T0A	R10	DVDD_MD1
AD2	BPI_BUS9	C14	CSI0A_L2N_T1C	R11	DVSS
AD20	DVSS	C16	CSI0A_L0P_T0A	R12	DVDD_SRAM_MODEM
AD21	DVDD_GPU	C18	CSI2B_L1P	R13	DVDD_MD1
AD22	DVDD_GPU	C2	DVSS	R14	DVDD_MD1
AD25	DVDD_GPU	C21	CSI2A_L1N	R15	DVSS
AD26	DVDD_GPU	C25	CSI1B_L0N	R16	DVSS
AD27	DVSS	C26	CSI1A_L1N	R17	DVDD_SRAM_MODEM
AD28	DVSS	C27	CSI1A_L1P	R18	DVDD_MD1
AD29	SCL2	C29	CAM_PDN2	R19	DVSS
AD3	BPI_BUS5	C3	RFIC_BSI_0_EN	R2	PRX_BB_I2
AD30	I2S2_BCK	C30	CAM_RST1	R20	DVDD_MD1
AD31	I2S2_LRCK	C31	JTRST_B	R21	DVDD_SRAM_TOP
AD32	KPCOL2	C32	JTMS	R22	DVDD_TOP
AD33	KPCOL1	C33	DVSS	R23	DVSS
AD34	UTXD1	C34	VDD1	R24	DVSS
AD5	RFU	C4	BPI_BUS15_VM1	R25	DVDD_TOP
AD8	DVSS	C5	BPI_BUS17_SWP1	R26	DVDD_TOP
AD9	DVDD_DVFS1	C6	MIPI6_SDATA	R27	DVSS
AE1	BPI_BUS2	C7	MIPI6_SCLK	R28	DVSS
AE10	DVDD_DVFS1	C8	MIPI5_SCLK	R29	DVSS
AE11	DVSS	C9	MIPI5_SDATA	R3	DVSS
AE12	DVSS	D1	VDD2	R32	DVSS
AE13	DVDD_DVFS2	D10	DVSS	R34	UFS_RST_N
AE14	DVDD_DVFS2	D11	CSI0B_L1P_T0C	R4	DVSS
AE15	DVDD_DVFS2	D13	CSI0B_L0N_T0B	R5	DET_IP1
AE16	DVSS	D14	CSI0A_L1N_T1A	R6	DVSS
AE17	DVDD_DVFS2	D15	DVSS	R9	DVDD_MD1
AE18	DVDD_TOP	D16	CSI0A_L0N_T0B	T1	DRX_BB_I2
AE19	DVSS	D17	DVSS	T10	DVDD_MD1
AE2	BPI_BUS3	D18	CSI2B_L1N	T11	DVSS
AE20	DVSS	D19	CSI2B_L0P	T12	DVDD_SRAM_MODEM
AE21	DVDD_GPU	D2	VDD2	T13	DVDD_MD1
AE22	DVDD_GPU	D21	CSI2A_L0P	T14	DVDD_MD1
AE25	DVDD_GPU	D22	CSI2A_L0N	T15	DVSS
AE26	DVDD_GPU	D23	DVSS	T16	DVSS
AE27	DVSS	D24	CSI1B_L1N	T17	DVDD_SRAM_MODEM
AE28	DVSS	D25	CSI1B_L1P	T18	DVDD_MD1
AE29	SDA2	D27	CSI1A_L0N	T19	DVSS
AE3	BPI_BUS1	D28	CSI1A_L0P	T2	PRX_BB_Q2
AE30	SDA1	D29	CAM_PDN1	T20	DVDD_SRAM_TOP
AE31	SCL1	D3	RFIC_BSI_0_CK	T21	DVDD_SRAM_TOP
AE32	KPROW2	D30	CAM_PDN0	T22	DVDD_TOP

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AE33	KPROW0	D31	MSDC3_DAT3	T23	DVSS
AE34	KPCOL0	D32	JTDO	T24	DVSS
AE4	EINT14	D33	VDD2	T25	DVDD_TOP
AE5	SPI3_MI	D34	VDD2	T26	DVDD_TOP
AE8	DVSS	D4	BPI_BUS16_SWP0	T27	DVSS
AE9	DVDD_DVFS1	D5	BPI_BUS18_SWP2	T28	DVSS
AF1	DVDD18_CPU	D7	MIPI4_SDATA	T29	MSDC0_DAT7
AF10	VDD2_B0_B	D8	MIPI4_SCLK	T3	DVSS
AF11	VDD2_CA_B	E1	TX_BB_IP0	T32	MSDC0_DAT2
AF12	VDD2_B1_B	E10	CM3MCLK	T33	MSDC0_DAT1
AF16	DVSS	E14	CSI0A_L1P_T0C	T4	DET_QP1
AF2	BPI_BUS0	E19	CSI2B_L0N	T5	DET_IN1
AF20	DVSS	E2	DVSS	T9	DVDD_MD1
AF21	DVDD_GPU	E20	CSI2A_L2P	U1	DRX_BB_Q2
AF22	DVDD_TOP	E21	CSI2A_L2N	U10	DVDD_MD1
AF23	VDD2_B1_D	E29	MSDC3_DSL	U11	DVSS
AF24	VDD2_CA_D	E3	AVDD18_MD	U12	DVDD_SRAM_MODEM
AF25	VDD2_B0_D	E30	MSDC3_CMD	U13	DVDD_MD1
AF26	DVDD_TOP	E31	MSDC3_DAT1	U14	DVDD_MD1
AF27	AVDD12_D	E32	MSDC3_DAT2	U15	DVSS
AF29	UTXD0	E33	MSDC3_DAT0	U16	DVSS
AF3	SCL5	E34	DVDD18_IOMC3	U17	DVDD_SRAM_MODEM
AF30	URXD0	E4	BPI_BUS19_SWP3	U18	DVDD_MD1
AF32	UTXD2	E5	DVDD_VQPS	U19	DVSS
AF34	KPROW1	E6	BPI_BUS20_DET0	U2	DVSS
AF4	EINT15	E7	BPI_BUS21_DET1	U20	DVDD_SRAM_TOP
AF5	SPI3_CS	F1	TX_BB_IN0	U21	DVDD_TOP
AF6	RFU	F2	TX_BB_QP0	U22	DVDD_TOP
AF7	DVDD18_IOETC	F29	MSDC3_CLK	U23	DVDD_GPU
AF8	AVDD12_B	F30	CLK_URXD	U24	DVDD_GPU
AF9	DVDD_TOP	F31	SH_URXD	U25	DVDD_GPU
AG1	AVDD18_USB	F32	SH_UTXD	U26	DVDD_GPU
AG10	VDDQ_B0_B	F33	UTXD3	U27	DVSS
AG11	VDDQ_CA_B	F34	DVDD18_IOBL	U28	DVSS
AG12	VDDQ_B1_B	F4	APC	U29	MSDC0_DAT6
AG16	DVSS	G10	DVSS	U30	MSDC0_DAT5
AG2	DVDD18_IOTR	G11	DVSS	U31	MSDC0_DAT4
AG20	DVDD_TOP	G12	VDDQ_B0_A	U32	DVSS
AG21	DVDD_GPU	G13	VDDQ_CA_A	U33	MSDC0_DAT0
AG22	DVSS	G14	VDDQ_B1_A	U34	MSDC0_DAT3
AG23	VDDQ_B1_D	G15	DVSS	U4	DET_QN1
AG24	VDDQ_CA_D	G2	TX_BB_QN0	U6	DVSS
AG25	VDDQ_B0_D	G20	DVSS	U7	DVSS
AG26	DVSS	G21	VDDQ_B1_C	U8	DVDD_SRAM_TOP_1
AG27	DVSS	G22	VDDQ_CA_C	U9	DVDD_MD1
AG29	SIM1_SIO	G23	VDDQ_B0_C	V10	DVSS
AG3	SDA5	G24	AVDD12_C	V11	DVSS
AG30	INT_SIM2	G25	DVSS	V12	DVSS
AG31	INT_SIM1	G26	DVDD_IPUSYS	V13	DVSS
AG32	URXD2	G27	DVSS	V14	DVSS

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AG33	SCL0	G28	DVSS	V15	DVSS
AG34	SDA0	G29	DSI1_TE	V16	DVSS
AG4	SPI3_CK	G3	DVSS	V17	DVDD_MD1
AG5	SPI3_MO	G30	CLK_UTXD	V18	DVDD_MD1
AG7	DVDD18_IOETC	G31	SDA3	V19	DVDD_SRAM_TOP
AG8	DVDD18_IOETC	G33	URXD3	V2	REFP
AG9	DVDD_TOP	G5	DVSS	V20	DVDD_SRAM_TOP
AH1	DVDD12_CPU	G6	RFIC_ET0_P	V21	DVDD_TOP
AH11	DVSS	G7	RFIC_ET0_N	V22	DVDD_TOP
AH12	DVSS	H1	PRX_BB_I0	V23	DVDD_GPU
AH2	AVDD09_SSUSB	H10	AVDD12_A	V24	DVDD_GPU
AH29	SIM1_SCLK	H11	DVDD_TOP	V25	DVDD_GPU
AH30	SIM2_SRST	H12	VDD2_B0_A	V26	DVDD_SRAM_GPU_2
AH31	SIM2_SIO	H13	VDD2_CA_A	V27	DVSS
AH32	SPI2_MO	H14	VDD2_B1_A	V28	DVSS
AH33	SPI2_CK	H15	DVDD_TOP	V29	VOW_CLK_MISO
AH34	SPI2_CS	H16	DVSS	V3	DVSS
AH4	DVSS	H17	DVSS	V30	AUD_CLK_MOSI
AH5	DVSS	H18	DVSS	V31	MSDC0_DSL
AJ1	AVDD12_USB	H19	DVSS	V32	MSDC0_RSTB
AJ16	TDM_DATA0	H2	DVSS	V33	MSDC0_CMD
AJ17	DPI_CK	H20	DVDD_TOP	V34	MSDC0_CLK
AJ18	DPI_VSYNC	H21	VDD2_B1_C	V4	DVSS
AJ19	DPI_D2	H22	VDD2_CA_C	V5	DVSS
AJ2	AVDD12_SSUSB	H23	VDD2_B0_C	V7	AUXIN1
AJ20	DPI_D0	H24	DVDD_TOP	V9	DVSS
AJ21	PWRAP_SPI0_CK	H25	DVSS	W1	AVDD12_MD
AJ22	SRCLKENAI1	H26	DVDD_IPUSYS	W11	DVSS
AJ23	SRCLKENAI0	H27	DVSS	W12	DVSS
AJ24	SYSRSTB	H28	DVSS	W13	DVSS
AJ25	SCL6	H29	LCM1_RST	W14	DVSS
AJ26	SDA6	H3	DVSS	W15	DVSS
AJ27	EINT0	H31	SCL3	W16	DVSS
AJ28	EINT1	H32	GPS_SYNC	W17	DVSS
AJ29	SIM1_SRST	H33	DAISYNC	W18	DVDD_SRAM_TOP
AJ3	DVSS	H34	EXT_FRAME_SYNC	W19	DVDD_SRAM_TOP
AJ30	SIM2_SCLK	H4	DVSS	W2	DVSS
AJ32	SPI2_MI	H6	DVSS	W20	DVSS
AJ34	DVDD28_MC2	J1	PRX_BB_Q0	W21	DVDD_GPU
AJ4	SSUSB_TXP	J10	DVSS	W22	DVDD_GPU
AJ5	DVSS	J11	DVSS	W23	DVDD_GPU
AJ6	USB_DP_P0	J12	DVSS	W24	DVDD_GPU
AK1	AVDD33_USB_P1	J13	DVSS	W25	DVDD_GPU
AK15	TDM_DATA2	J14	DVSS	W26	DVDD_SRAM_GPU_2
AK17	DPI_DE	J15	DVSS	W27	DVSS
AK18	DPI_HSYNC	J16	DVSS	W28	DVSS
AK2	AVDD33_USB_P0	J17	DVDD_MODEM	W29	SPI1_CK
AK20	DPI_D1	J18	DVDD_MODEM	W3	AUXIN0
AK21	DPI_D4	J19	DVSS	W30	AUD_DAT_MISO1
AK22	PWRAP_SPI0_MO	J2	DRX_BB_I0	W31	AUD_DAT_MISO2

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AK23	DISP_PWM0	J20	DVSS	W32	AUD_DAT_MOSI1
AK24	SRCLKENA1	J21	DVDD_TOP	W33	AUD_DAT_MOSI2
AK25	PMIC_MFG_BOOST	J22	DVDD_TOP	W34	DVDD18_MSDC0
AK26	SDA4	J23	DVSS	W4	AUXIN3
AK27	SCL4	J24	DVSS	W6	AUXIN2
AK28	EINT2	J25	DVSS	Y1	AVDD18_AP
AK29	EINT3	J26	DVDD_IPUSYS	Y11	DVSS
AK3	SSUSB_TXN	J27	DVDD_IPUSYS	Y12	DVSS
AK31	DVDD28_MC1	J28	DVSS	Y13	DVDD_DVFS1
AK32	DVDD28_SIM1	J29	PTA_UTXD	Y14	DVSS
AK33	DVDD28_SIM2	J3	DVSS	Y15	AVDD09_PLLGP
AK34	DVDD18_MC2	J30	PTA_URXD	Y16	PLLGP_TP
AK5	DVSS	J32	DAIPCMIN	Y17	DVSS
AK6	USB_DM_P0	J33	DAIPCMOUT	Y18	DVDD_SRAM_TOP
AK7	DVSS	J34	DAICLK	Y19	DVSS
AK8	DSI1_CKP	J5	DVSS	Y2	RFIC_BSI_1_D2
AK9	DSI1_CKN	J6	MAIN_X26M_IN	Y20	DVSS
AL1	VDD2	J9	DVSS	Y21	DVDD_SRAM_GPU_1
AL10	DSI1_D3P	K10	DVDD_MODEM	Y22	DVDD_GPU
AL11	DSI1_D3N	K11	DVSS	Y23	DVSS
AL12	DSI0_D1N	K12	DVSS	Y24	DVSS
AL13	DSI0_D3P	K13	DVDD_MODEM	Y25	DVDD_GPU
AL14	DSI0_D3N	K14	DVDD_MODEM	Y26	DVDD_SRAM_GPU_2
AL15	TDM_DATA3	K15	DVSS	Y27	DVSS
AL16	TDM_MCK	K16	DVSS	Y28	DVSS
AL17	TDM_LRCK	K17	DVDD_MODEM	Y29	SPI1_MI
AL18	DPI_D9	K18	DVDD_MODEM	Y30	SPI1_CS
AL19	DPI_D10	K19	DVSS	Y32	I2S1_BCK
AL2	VDD2	K2	DRX_BB_Q0	Y34	DVDD12_IOAUD
AL20	DPI_D11	K20	DVDD_MODEM	Y4	AUXIN4
AL21	PWRAP_SPI0_CSN	K21	DVDD_TOP	Y6	MIPI1_SDATA
AL22	PWRAP_SPI0_MI	K22	DVDD_TOP	Y7	I2S1_MCK

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-3. Detailed pin description

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	DVDD18_IORB
WATCHDOG	DIO	Watchdog reset output	DVDD18_IORB
TESTMODE	DIO	Test mode	DVDD18_IOBR
SRCLKENA0	DIO	26MHz co-clock enable output	DVDD18_IORB
SRCLKENA1	DIO	26MHz co-clock enable output	DVDD18_IORB
SRCLKENAI0	DIO	26MHz co-clock enable input	DVDD18_IORB
SRCLKENAI1	DIO	26MHz co-clock enable input	DVDD18_IORB
RTC32K_CK	DIO	32K clock input	DVDD18_IORB
PMIC			
PWRAP_SPI0_CK	DIO	PMIC SPI control interface	DVSS18_IORB
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVSS18_IORB
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVSS18_IORB
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVSS18_IORB
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD12_IOAUD
VOW_CLK_MISO	DIO	PMIC audio input interface	DVDD12_IOAUD
AUD_DAT_MISO1	DIO	PMIC audio input interface	DVDD12_IOAUD
AUD_DAT_MOSI1	DIO	PMIC audio input interface	DVDD12_IOAUD
AUD_DAT_MISO2	DIO	PMIC audio input interface	DVDD12_IOAUD
AUD_DAT_MOSI2	DIO	PMIC audio input interface	DVDD12_IOAUD
SIM			
SIM1_SCLK	DIO	SIM1 clock	VDD18_SIM VDD28_SIM1
SIM1_SIO	DIO	SIM1 data	VDD18_SIM VDD28_SIM1
SIM1_SRST	DIO	SIM1 RST	VDD18_SIM VDD28_SIM1
SIM2_SCLK	DIO	SIM2 clock	VDD18_SIM VDD28_SIM2
SIM2_SIO	DIO	SIM2 data	VDD18_SIM VDD28_SIM2
SIM2_SRST	DIO	SIM2 RST	VDD18_SIM VDD28_SIM2
INT_SIM1	DIO	SIM1 INT	DVDD18_IOBR
INT_SIM2	DIO	SIM2 INT	DVDD18_IOBR
JTAG			
JTCK	DIO	JTCK	DVDD18_IOLB
JTDI	DIO	JTDI	DVDD18_IOLB
JTDO	DIO	JTDO	DVDD18_IOLB
JTMS	DIO	JTMS	DVDD18_IOLB
JTRST_B	DIO	JTRST	DVDD18_IOLB
LCD			
DISP_PWM0	DIO	Display PWM output	DVSS18_IORB
DSI_TE	DIO	Parallel display interface tearing effect	DVSS18_IORB

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Pin name	Type	Description	Power domain
LCM_RST	DIO	Parallel display interface reset signal	DVSS18_IORB
I2S			
I2S1_MCK	DIO	I2S interface	DVDD18_IOTR
I2S1_BCK	DIO	I2S interface	DVDD18_IOBR
I2S1_DO0	DIO	I2S interface	DVDD18_IOBR
I2S1_DO1	DIO	I2S interface	DVDD18_IOBR
I2S1_LRCK	DIO	I2S interface	DVDD18_IOBR
I2S2_BCK	DIO	I2S interface	DVDD18_IOBR
I2S2_DI1	DIO	I2S interface	DVDD18_IOBR
I2S2_DI2	DIO	I2S interface	DVDD18_IOBR
I2S2_LRCK	DIO	I2S interface	DVDD18_IOBR
I2S2_MCK	DIO	I2S interface	DVDD18_IOBR
EINT			
EINT0	DIO	External interrupt 0	DVDD18_IORB
EINT1	DIO	External interrupt 1	DVDD18_IORB
EINT2	DIO	External interrupt 2	DVDD18_IORB
EINT3	DIO	External interrupt 3	DVDD18_IORB
EINT4	DIO	External interrupt 4	DVDD18_IORB
EINT5	DIO	External interrupt 5	DVDD18_IORB
EINT6	DIO	External interrupt 6	DVDD18_IORB
EINT7	DIO	External interrupt 7	DVDD18_IORB
EINT8	DIO	External interrupt 8	DVDD18_IORB
EINT9	DIO	External interrupt 9	DVDD18_IORB
EINT10	DIO	External interrupt 10	DVDD18_IORB
EINT11	DIO	External interrupt 11	DVDD18_IORB
EINT12	DIO	External interrupt 12	DVDD18_IORB
EINT13	DIO	External interrupt 13	DVDD18_IORB
EINT14	DIO	External interrupt 14	DVDD18_IOTR
EINT15	DIO	External interrupt 15	DVDD18_IOTR
SPI			
SPI0_CK	DIO	SPI clock	DVDD18_IOBR
SPI0_CS	DIO	SPI chip select	DVDD18_IOBR
SPI0_MI	DIO	SPI master data in	DVDD18_IOBR
SPI0_MO	DIO	SPI master data out	DVDD18_IOBR
SPI1_CK	DIO	SPI clock	DVDD18_IOBR
SPI1_CS	DIO	SPI chip select	DVDD18_IOBR
SPI1_MI	DIO	SPI master data in	DVDD18_IOBR
SPI1_MO	DIO	SPI master data out	DVDD18_IOBR
RF Interface			
BPI_BUS0	DIO	BPI_BUS0	DVDD18_IOTR
BPI_BUS1	DIO	BPI_BUS1	DVDD18_IOTR
BPI_BUS2	DIO	BPI_BUS2	DVDD18_IOTR
BPI_BUS3	DIO	BPI_BUS3	DVDD18_IOTR

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Pin name	Type	Description	Power domain
BPI_BUS4	DIO	BPI_BUS4	DVDD18_IOTR
BPI_BUS5	DIO	BPI_BUS5	DVDD18_IOTR
BPI_BUS6	DIO	BPI_BUS6	DVDD18_IOTR
BPI_BUS7	DIO	BPI_BUS7	DVDD18_IOTR
BPI_BUS8	DIO	BPI_BUS8	DVDD18_IOTR
BPI_BUS9	DIO	BPI_BUS9	DVDD18_IOTR
BPI_BUS10	DIO	BPI_BUS10	DVDD18_IOTR
BPI_BUS11	DIO	BPI_BUS11	DVDD18_IOTR
BPI_BUS12	DIO	BPI_BUS12	DVDD18_IOTR
BPI_BUS13	DIO	BPI_BUS13	DVDD18_IOTR
BPI_BUS14_VM0	DIO	BPI_BUS14_VM0	DVDD18_IOLT
BPI_BUS15_VM1	DIO	BPI_BUS15_VM1	DVDD18_IOLT
BPI_BUS16_SWP0	DIO	BPI_BUS16_SWP0	DVDD18_IOLT
BPI_BUS17_SWP1	DIO	BPI_BUS17_SWP1	DVDD18_IOLT
BPI_BUS18_SWP2	DIO	BPI_BUS18_SWP2	DVDD18_IOLT
BPI_BUS19_SWP3	DIO	BPI_BUS19_SWP3	DVDD18_IOLT
BPI_BUS20_DET0	DIO	BPI_BUS20_DET0	DVDD18_IOLT
BPI_BUS21_DET1	DIO	BPI_BUS21_DET1	DVDD18_IOLT
RFIC_BSI_0_EN	DIO	RFIC0 BSI DATA0	DVDD18_IOLT
RFIC_BSI_0_CK	DIO	RFIC0 BSI DATA1	DVDD18_IOLT
RFIC_BSI_0_D0	DIO	RFIC0 BSI DATA2	DVDD18_IOLT
RFIC_BSI_0_D1	DIO	RFIC0 BSI CS0	DVDD18_IOLT
RFIC_BSI_0_D2	DIO	RFIC0 BSI CLK	DVDD18_IOLT
RFIC_BSI_1_EN	DIO	RFIC1 BSI CLK	DVDD18_IOTR
RFIC_BSI_1_CK	DIO	RFIC1 BSI DATA0	DVDD18_IOTR
RFIC_BSI_1_D0	DIO	RFIC1 BSI DATA1	DVDD18_IOTR
RFIC_BSI_1_D1	DIO	RFIC1 BSI DATA2	DVDD18_IOTR
RFIC_BSI_1_D2	DIO	RFIC1 BSI CS0	DVDD18_IOTR
MIPI0_SDATA	DIO	MISC BSI CLK	DVDD18_IOLT
MIPI0_SCLK	DIO	MISC BSI CS0	DVDD18_IOLT
MIPI1_SDATA	DIO	MISC BSI CLK	DVDD18_IOTR
MIPI1_SCLK	DIO	MISC BSI CS0	DVDD18_IOTR
MIPI2_SDATA	DIO	MISC BSI CS1	DVDD18_IOTR
MIPI2_SCLK	DIO	MISC BSI DATAI	DVDD18_IOTR
MIPI3_SDATA	DIO	MISC BSI DATAO	DVDD18_IOTR
MIPI3_SCLK	DIO	TXBPI	DVDD18_IOTR
MIPI4_SDATA	DIO	MISC BSI CLK	DVDD18_IOLT
MIPI4_SCLK	DIO	MISC BSI CS0	DVDD18_IOLT
MIPI5_SDATA	DIO	MISC BSI CS1	DVDD18_IOLT
MIPI5_SCLK	DIO	MISC BSI DATAI	DVDD18_IOLT
MIPI6_SDATA	DIO	MISC BSI DATAO	DVDD18_IOLT
MIPI6_SCLK	DIO	TXBPI	DVDD18_IOLT
MIPI7_SDATA	DIO	MISC BSI DATAO	DVDD18_IOLT

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Pin name	Type	Description	Power domain
MIPI7_SCLK	DIO	TXBPI	DVDD18_IOLT
MSDC0			
MSDC0_CLK	DIO	MSDC0 CLK	DVDD18_MSDC0
MSDC0_CMD	DIO	MSDC0 CMD	DVDD18_MSDC0
MSDC0_DAT0	DIO	MSDC0 data 0 pin	DVDD18_MSDC0
MSDC0_DAT1	DIO	MSDC0 data 1 pin	DVDD18_MSDC0
MSDC0_DAT2	DIO	MSDC0 data 2 pin	DVDD18_MSDC0
MSDC0_DAT3	DIO	MSDC0 data 3 pin	DVDD18_MSDC0
MSDC0_DAT4	DIO	MSDC0 data 4 pin	DVDD18_MSDC0
MSDC0_DAT5	DIO	MSDC0 data 5 pin	DVDD18_MSDC0
MSDC0_DAT6	DIO	MSDC0 data 6 pin	DVDD18_MSDC0
MSDC0_DAT7	DIO	MSDC0 data 7 pin	DVDD18_MSDC0
MSDC0_DSL	DIO	MSDC0 DSL	DVDD18_MSDC0
MSDC0_RST_	DIO	MSDC0 RST	DVDD18_MSDC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD18_MC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD18_MC1
MSDC1_DAT0	DIO	MSDC1 data 0 pin	DVDD18_MC1
MSDC1_DAT1	DIO	MSDC1 data 1 pin	DVDD18_MC1
MSDC1_DAT2	DIO	MSDC1 data 2 pin	DVDD18_MC1
MSDC1_DAT3	DIO	MSDC1 data 3 pin	DVDD18_MC1
MSDC3			
MSDC3_CLK	DIO	MSDC3 clock output	DVDD18_IOMC3
MSDC3_CMD	DIO	MSDC3 command pin	DVDD18_IOMC3
MSDC3_DAT0	DIO	MSDC3 data 0 pin	DVDD18_IOMC3
MSDC3_DAT1	DIO	MSDC3 data 1 pin	DVDD18_IOMC3
MSDC3_DAT2	DIO	MSDC3 data 2 pin	DVDD18_IOMC3
MSDC3_DAT3	DIO	MSDC3 data 3 pin	DVDD18_IOMC3
CAM			
CM0MCLK	DIO	Digital camera interface	DVDD18_IOLT
CM1MCLK	DIO	Digital camera interface	DVDD18_IOLT
CM2MCLK	DIO	Digital camera interface	DVDD18_IOLT
CM3MCLK	DIO	Digital camera interface	DVDD18_IOLT
I2C			
SCL0	DIO	I2C0 clock	DVDD18_IOBR
SDA0	DIO	I2C0 data	DVDD18_IOBR
SCL1	DIO	I2C1 clock	DVDD18_IOBR
SDA1	DIO	I2C1 data	DVDD18_IOBR
SCL2	DIO	I2C2 clock	DVDD18_IOBR
SDA2	DIO	I2C2 data	DVDD18_IOBR
SCL3	DIO	I2C3 clock	DVDD18_IOBL
SDA3	DIO	I2C3 data	DVDD18_IOBL
SCL4	DIO	I2C4 clock	DVDD18_IORB

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Pin name	Type	Description	Power domain
SDA4	DIO	I2C4 data	DVDD18_IORB
SCL5	DIO	I2C5 clock	DVDD18_IOTR
SDA5	DIO	I2C5 data	DVDD18_IOTR
SCL6	DIO	I2C6 clock	DVDD18_IORB
SDA6	DIO	I2C6 data	DVDD18_IORB
SCL7	DIO	I2C7 clock	DVDD18_IORB
SDA7	DIO	I2C7 data	DVDD18_IORB
UART			
URXD0	DIO	UART0 RX	DVDD18_IOBR
UTXD0	DIO	UART0 TX	DVDD18_IOBR
URXD1	DIO	UART1 RX	DVDD18_IOBR
UTXD1	DIO	UART1 TX	DVDD18_IOBR
URXD2	DIO	UART2 RX	DVDD18_IOBR
UTXD2	DIO	UART2 TX	DVDD18_IOBR
URXD3	DIO	UART3 RX	DVDD18_IOBL
UTXD3	DIO	UART3 TX	DVDD18_IOBL
Keypad			
KPCOL0	DIO	Keypad COL0	DVDD18_IOBR
KPCOL1	DIO	Keypad COL1	DVDD18_IOBR
KPCOL2	DIO	Keypad COL2	DVDD18_IOBR
KPROW0	DIO	Keypad ROW0	DVDD18_IOBR
KPROW1	DIO	Keypad ROW0	DVDD18_IOBR
KPROW2	DIO	Keypad ROW0	DVDD18_IOBR
DAI Merged Interface			
DAICLK	DIO	DAI audio interface	DVDD18_IOBL
DAIPCMIN	DIO	DAI audio interface	DVDD18_IOBL
DAIPCMOUT	DIO	DAI audio interface	DVDD18_IOBL
DAISYNC	DIO	DAI audio interface	DVDD18_IOBL
DPI			
DPI_CK	DIO	DPI clock	DVDD18_IORB
DPI_D0	DIO	DPI data 0	DVDD18_IORB
DPI_D1	DIO	DPI data 1	DVDD18_IORB
DPI_D2	DIO	DPI data 2	DVDD18_IORB
DPI_D3	DIO	DPI data 3	DVDD18_IORB
DPI_D4	DIO	DPI data 4	DVDD18_IORB
DPI_D5	DIO	DPI data 5	DVDD18_IORB
DPI_D6	DIO	DPI data 6	DVDD18_IORB
DPI_D7	DIO	DPI data 7	DVDD18_IORB
DPI_D8	DIO	DPI data 8	DVDD18_IORB
DPI_D9	DIO	DPI data 9	DVDD18_IORB
DPI_D10	DIO	DPI data 10	DVDD18_IORB
DPI_D11	DIO	DPI data11	DVDD18_IORB
DPI_DE	DIO	DPI data enable	DVDD18_IORB

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Pin name	Type	Description	Power domain
DPI_HSYNC	DIO	DPI HSYNC	DVDD18_IORB
DPI_VSYNC	DIO	DPI VSYNC	DVDD18_IORB
ABB			
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
AUXIN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUXIN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUXIN2	AIO	AuxADC external input channel 2	AVDD18_AP
AUXIN3	AIO	AuxADC external input channel 3	AVDD18_AP
AUXIN4	AIO	AuxADC external input channel 4	AVDD18_AP
DRX_BB_Q2	AIO	Diverse downlink Q-ch for path 2	AVDD18_MD
DRX_BB_I2	AIO	Diverse downlink I-ch for path 2	AVDD18_MD
PRX_BB_Q2	AIO	Main downlink Q-ch for path 2	AVDD18_MD
PRX_BB_I2	AIO	Main downlink I-ch for path 2	AVDD18_MD
DET_QN1	AIO	RF1 QN detection path	AVDD18_MD
DET_QP1	AIO	RF1 QP detection path	AVDD18_MD
DET_IN1	AIO	RF1 IN detection path	AVDD18_MD
DET_IP1	AIO	RF1 IP detection path	AVDD18_MD
TX_BB_QN1	AIO	Uplink QN for path1	AVDD18_MD
TX_BB_QP1	AIO	Uplink QP for path1	AVDD18_MD
TX_BB_IN1	AIO	Uplink IN for path1	AVDD18_MD
TX_BB_IP1	AIO	Uplink IP for path1	AVDD18_MD
RFIC_ET1_N	AIO	Envelop tracking DAC1 output P	AVDD18_MD
RFIC_ET1_P	AIO	Envelop tracking DAC1 output N	AVDD18_MD
MAIN_X26M_IN	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
RX_REF	AIO	Voltage reference	AVDD18_MD
DRX_BB_Q1	AIO	Diverse downlink Q-ch for path 1	AVDD18_MD
DRX_BB_I1	AIO	Diverse downlink I-ch for path 1	AVDD18_MD
PRX_BB_Q1	AIO	Main downlink Q-ch for path 1	AVDD18_MD
PRX_BB_I1	AIO	Main downlink I-ch for path 1	AVDD18_MD
DRX_BB_Q0	AIO	Diverse downlink Q-ch for path 0	AVDD18_MD
DRX_BB_I0	AIO	Diverse downlink I-ch for path 0	AVDD18_MD
PRX_BB_Q0	AIO	Main downlink Q-ch for path 0	AVDD18_MD
PRX_BB_I0	AIO	Main downlink I-ch for path 0	AVDD18_MD
DET_QN0	AIO	RF0 QN detection path	AVDD18_MD
DET_QP0	AIO	RF0 QP detection path	AVDD18_MD
DET_IN0	AIO	RF0 IN detection path	AVDD18_MD
DET_IP0	AIO	RF0 IP detection path	AVDD18_MD
TX_BB_QN0	AIO	Uplink QN for path0	AVDD18_MD
TX_BB_QP0	AIO	Uplink QP for path0	AVDD18_MD
TX_BB_IN0	AIO	Uplink IN for path0	AVDD18_MD
TX_BB_IP0	AIO	Uplink IP for path0	AVDD18_MD
RFIC_ET0_N	AIO	Envelop tracking DAC0 output P	AVDD18_MD
RFIC_ET0_P	AIO	Envelop tracking DAC0 output N	AVDD18_MD

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Pin name	Type	Description	Power domain
APC	AIO	Automatic power control	AVDD18_MD
MIPIRX			
CSI0B_L2N_T1C	AIO	CSI0B lane2 N	AVDD18_CSI AVDD12_CSI
CSI0B_L2P_T1B	AIO	CSI0B lane2 P	AVDD18_CSI AVDD12_CSI
CSI0B_L1N_T1A	AIO	CSI0B lane1 N	AVDD18_CSI AVDD12_CSI
CSI0B_L1P_T0C	AIO	CSI0B lane1 P	AVDD18_CSI AVDD12_CSI
CSI0B_L0N_T0B	AIO	CSI0B lane0 N	AVDD18_CSI AVDD12_CSI
CSI0B_L0P_T0A	AIO	CSI0B lane0 P	AVDD18_CSI AVDD12_CSI
CSI0A_L2N_T1C	AIO	CSI0A lane2 N	AVDD18_CSI AVDD12_CSI
CSI0A_L2P_T1B	AIO	CSI0A lane2 P	AVDD18_CSI AVDD12_CSI
CSI0A_L1N_T1A	AIO	CSI0A lane1 N	AVDD18_CSI AVDD12_CSI
CSI0A_L1P_T0C	AIO	CSI0A lane1 P	AVDD18_CSI AVDD12_CSI
CSI0A_L0N_T0B	AIO	CSI0A lane0 N	AVDD18_CSI AVDD12_CSI
CSI0A_L0P_T0A	AIO	CSI0A lane0 P	AVDD18_CSI AVDD12_CSI
CSI2B_L1P	AIO	CSI2B lane1 P	AVDD18_CSI AVDD12_CSI
CSI2B_L1N	AIO	CSI2B lane1 N	AVDD18_CSI AVDD12_CSI
CSI2B_L0P	AIO	CSI2B lane0 P	AVDD18_CSI AVDD12_CSI
CSI2B_L0N	AIO	CSI2B lane0 N	AVDD18_CSI AVDD12_CSI
CSI2A_L2P	AIO	CSI2A lane2 P	AVDD18_CSI AVDD12_CSI
CSI2A_L2N	AIO	CSI2A lane2 N	AVDD18_CSI AVDD12_CSI
CSI2A_L1P	AIO	CSI2A lane1 P	AVDD18_CSI AVDD12_CSI
CSI2A_L1N	AIO	CSI2A lane1 N	AVDD18_CSI AVDD12_CSI
CSI2A_L0P	AIO	CSI2A lane0 P	AVDD18_CSI AVDD12_CSI
CSI2A_L0N	AIO	CSI2A lane0 N	AVDD18_CSI AVDD12_CSI

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Pin name	Type	Description	Power domain
CSI1B_L2P	AIO	CSI1B lane2 P	AVDD18_CSI AVDD12_CSI
CSI1B_L2N	AIO	CSI1B lane2 N	AVDD18_CSI AVDD12_CSI
CSI1B_L1P	AIO	CSI1B lane1 P	AVDD18_CSI AVDD12_CSI
CSI1B_L1N	AIO	CSI1B lane1 N	AVDD18_CSI AVDD12_CSI
CSI1B_L0P	AIO	CSI1B lane0 P	AVDD18_CSI AVDD12_CSI
CSI1B_L0N	AIO	CSI1B lane0 N	AVDD18_CSI AVDD12_CSI
CSI1A_L2P	AIO	CSI1A lane2 P	AVDD18_CSI AVDD12_CSI
CSI1A_L2N	AIO	CSI1A lane2 N	AVDD18_CSI AVDD12_CSI
CSI1A_L1P	AIO	CSI1A lane1 P	AVDD18_CSI AVDD12_CSI
CSI1A_L1N	AIO	CSI1A lane1 N	AVDD18_CSI VDD12_CSI
USB2			
USB_DP_P0	AIO	USB port0 D+ differential data line	AVDD33_USB
USB_DM_P0	AIO	USB port0 D- differential data line	AVDD33_USB
USB_DP_P1	AIO	USB port1 D+ differential data line	AVDD33_USB
USB_DM_P1	AIO	USB port1 D- differential data line	AVDD33_USB
CHD_DM_P0	AIO	BC1.1 charger DM	AVDD33_USB
CHD_DP_P0	AIO	BC1.1 charger DP	AVDD33_USB
USB3			
SSUSB_RXN	AIO	SSUSB RXDATA	AVDD10_SSUSB
SSUSB_RXP	AIO	SSUSB RXDATA	AVDD10_SSUSB
SSUSB_TXN	AIO	SSUSB TXDATA	AVDD10_SSUSB
SSUSB_TXP	AIO	SSUSB TXDATA	AVDD10_SSUSB
UFS			
UFS_RST_N	AIO	UFS reset	AVDD12_UFS
UFS_TX0N	AIO	UFS TX N	AVDD12_UFS
UFS_TX0P	AIO	UFS TX P	AVDD12_UFS
UFS_RX0N	AIO	UFS RX N	AVDD12_UFS
UFS_RX0P	AIO	UFS RX P	AVDD12_UFS
MIPITX			
DSI1_D3N_XXX	AIO	DSI1 lane 3 N	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D3P_T2C	AIO	DSI1 lane 3 P	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D1N_T2B	AIO	DSI1 lane 1 N	AVDD04_DSI1

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Pin name	Type	Description	Power domain
			AVDD12_DSI1 AVDD18_DSI1
DSI1_D1P_T2A	AIO	DSI1 lane 1 P	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_CKN_T1C	AIO	DSI1 CK lane N	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_CKP_T1B	AIO	DSI1 CK lane P	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D0N_T1A	AIO	DSI1 lane 0 N	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D0P_T0C	AIO	DSI1 lane 0 P	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D2N_T0B	AIO	DSI1 lane 2 N	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI1_D2P_T0A	AIO	DSI1 lane 2 P	AVDD04_DSI1 AVDD12_DSI1 AVDD18_DSI1
DSI0_D3N_XXX	AIO	DSI0 lane 3 N	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D3P_T2C	AIO	DSI0 lane 3 P	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D1N_T2B	AIO	DSI0 lane 1 N	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D1P_T2A	AIO	DSI0 lane 1 P	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_CKN_T1C	AIO	DSI0 CK lane N	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_CKP_T1B	AIO	DSI0 CK lane P	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D0N_T1A	AIO	DSI0 lane 0 N	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D0P_T0C	AIO	DSI0 lane 0 P	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D2N_T0B	AIO	DSI0 lane 2 N	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
DSI0_D2P_T0A	AIO	DSI0 lane 2 P	AVDD04_DSI0 AVDD12_DSI0 AVDD18_DSI0
PLL			
PLLGP_TP	AIO	PLL testpin P	AVDD18_ARMPLL

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Pin name	Type	Description	Power domain
PLLGP_TN	AIO	PLL testpin T	AVDD18_ARMPLL
Analog Power/Ground			
AVDD12_SSUSB	P	Analog power 1.2V for SSUSB	
AVDD09_SSUSB	P	Analog power 0.9V for SSUSB	
AVDD33_USB_P1	P	Analog power 3.3V for USB	
AVDD12_USB_P1	P	Analog power 1.2V for USB	
AVDD18_USB_P1	P	Analog power 1.8V for USB	
AVDD33_USB_P0	P	Analog power 3.3V for USB	
AVDD12_USB_P0	P	Analog power 1.2V for USB	
AVDD18_USB_P0	P	Analog power 1.8V for USB	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD12_PLLGP	P	Analog power input 1.2V for PLL	
AVDD09_PLLGP	P	Analog power input 0.9V for PLL	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX	
AVDD12_CSI	P	Analog power for MIPI CSI	
AVDD18_CSI	P	Analog power for MIPI CSI	
AVDD09_UFS	P	Analog power 0.9V for UFS	
AVDD12_UFS	P	Analog power 1.2V for UFS	
AVDD18_UFS	P	Analog power 1.8V for UFS	
AVDD04_DSI1	P	Analog power for DSI1	
AVDD12_DSI1	P	Analog power 1.2V for DSI1	
AVDD18_DSI1	P	Analog power 1.8V for DSI1	
AVDD04_DSI0	P	Analog power for DSI0	
AVDD12_DSI0	P	Analog power 1.2V for DSI0	
AVDD18_DSI0	P	Analog power 1.8V for DSI0	
AVSS_SSUSB	P	Analog ground for SSUSB	
AVSS33_USB_P1	P	Analog ground 3.3V for USB	
AVSS_USB	P	Analog ground for USB	
AVSS33_USB_P0	P	Analog ground 3.3V for USB	
AVSS_PLLGP	P	Analog ground for PLL	
AVSS_MD	P	Analog ground for BBTX, BBRX	
AVSS12_CSI	P	Analog ground for MIPI CSI	
AVSS_UFS	P	Analog ground for UFS	
AVSS12_DSI1	P	Analog ground for DSI1	
AVSS12_DSI0	P	Analog ground for DSI0	
DDR Power			
DDRV_A	P	DRAM I/O power	
DDRV_B	P	DRAM I/O power	
DDRVPOP	P	DRAM I/O power	
EXTDN_A		DRAM REXTDN pin	
VBIASN1_A	P	DRAM VBIASN power	-
VBIASN1_B	P	DRAM VBIASN power	-

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Pin name	Type	Description	Power domain
VBIASNPOP	P	DRAM VBIASN power	-
VDD1	P	DRAM VDD1 core power	-
VDDQ	P	DRAM I/O power	-
VREF(CA)_A	P	DRAM VREF(CA) power	-
VREF(CA)_B	P	DRAM VREF(CA) power	-
VREF(DQ)_A	P	DRAM VREF(DQ) power	-
VREF(DQ)_B	P	DRAM VREF(DQ) power	-
VREF_A	P	DRAM VREF power	-
VREF_B	P	DRAM VREF power	-
ZQ0_A		DRAM channel A reference pin 0 for output drive strength calibration	
ZQ0_B		DRAM channel B reference pin 0 for output drive strength calibration	
ZQ1_A		DRAM channel A reference pin 1 for output drive strength calibration	
ZQ1_B		DRAM channel B reference pin 0 for output drive strength calibration	
DDR IO			
CAPOP0_A	DIO	DRAM channel A address output 0	DDRVPOP
CAPOP1_A	DIO	DRAM channel A address output 1	DDRVPOP
CAPOP2_A	DIO	DRAM channel A address output 2	DDRVPOP
CA0_A	DIO	DRAM channel A address output 0	VDDQ_CA_A
CA1_A	DIO	DRAM channel A address output 1	VDDQ_CA_A
CA2_A	DIO	DRAM channel A address output 2	VDDQ_CA_A
CA3_A	DIO	DRAM channel A address output 3	VDDQ_CA_A
CA4_A	DIO	DRAM channel A address output 4	VDDQ_CA_A
CA5_A	DIO	DRAM channel A address output 5	VDDQ_CA_A
CKE0_A	DIO	DRAM channel A command output CKE 0	VDDQ_CA_A
CKE1_A	DIO	DRAM channel A command output CKE 1	VDDQ_CA_A
CK_T_A	DIO	DRAM channel A clock 0 output	VDDQ_CA_A
CK_C_A	DIO	DRAM channel A clock 0 output #	VDDQ_CA_A
CS0_A	DIO	DRAM channel A chip select 0 #	VDDQ_CA_A
CS1_A	DIO	DRAM channel A chip select 1 #	VDDQ_CA_A
DQ0_A	DIO	DRAM channel A data pin 0	VDDQ_B0_A
DQ1_A	DIO	DRAM channel A data pin 1	VDDQ_B0_A
DQ2_A	DIO	DRAM channel A data pin 2	VDDQ_B0_A
DQ3_A	DIO	DRAM channel A data pin 3	VDDQ_B0_A
DQ4_A	DIO	DRAM channel A data pin 4	VDDQ_B0_A
DQ5_A	DIO	DRAM channel A data pin 5	VDDQ_B0_A
DQ6_A	DIO	DRAM channel A data pin 6	VDDQ_B0_A
DQ7_A	DIO	DRAM channel A data pin 7	VDDQ_B0_A
DQ8_A	DIO	DRAM channel A data pin 8	VDDQ_B1_A
DQ9_A	DIO	DRAM channel A data pin 9	VDDQ_B1_A
DQ10_A	DIO	DRAM channel A data pin 10	VDDQ_B1_A

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Pin name	Type	Description	Power domain
DQ11_A	DIO	DRAM channel A data pin 11	VDDQ_B1_A
DQ12_A	DIO	DRAM channel A data pin 12	VDDQ_B1_A
DQ13_A	DIO	DRAM channel A data pin 13	VDDQ_B1_A
DQ14_A	DIO	DRAM channel A data pin 14	VDDQ_B1_A
DQ15_A	DIO	DRAM channel A data pin 15	VDDQ_B1_A
DMI0_A	DIO	DRAM channel A DQM 0	VDDQ_B0_A
DMI1_A	DIO	DRAM channel A DQM 1	VDDQ_B1_A
DQS0_T_A	DIO	DRAM channel A DQS 0	VDDQ_B0_A
DQS0_C_A	DIO	DRAM channel A DQS 0 #	VDDQ_B0_A
DQS1_T_A	DIO	DRAM channel A DQS 1	VDDQ_B1_A
DQS1_C_A	DIO	DRAM channel A DQS 1 #	VDDQ_B1_A
CA0_B	DIO	DRAM channel B address output 0	VDDQ_CA_B
CA1_B	DIO	DRAM channel B address output 1	VDDQ_CA_B
CA2_B	DIO	DRAM channel B address output 2	VDDQ_CA_B
CA3_B	DIO	DRAM channel B address output 3	VDDQ_CA_B
CA4_B	DIO	DRAM channel B address output 4	VDDQ_CA_B
CA5_B	DIO	DRAM channel B address output 5	VDDQ_CA_B
CKE0_B	DIO	DRAM channel B command output CKE 0	VDDQ_CA_B
CKE1_B	DIO	DRAM channel B command output CKE 1	VDDQ_CA_B
CK_T_B	DIO	DRAM channel B clock 0 output	VDDQ_CA_B
CK_C_B	DIO	DRAM channel B clock 0 output #	VDDQ_CA_B
CS0_B	DIO	DRAM channel B chip select 0 #	VDDQ_CA_B
CS1_B	DIO	DRAM channel B chip select 1 #	VDDQ_CA_B
DQ0_B	DIO	DRAM channel B data pin 0	VDDQ_B0_B
DQ1_B	DIO	DRAM channel B data pin 1	VDDQ_B0_B
DQ2_B	DIO	DRAM channel B data pin 2	VDDQ_B0_B
DQ3_B	DIO	DRAM channel B data pin 3	VDDQ_B0_B
DQ4_B	DIO	DRAM channel B data pin 4	VDDQ_B0_B
DQ5_B	DIO	DRAM channel B data pin 5	VDDQ_B0_B
DQ6_B	DIO	DRAM channel B data pin 6	VDDQ_B0_B
DQ7_B	DIO	DRAM channel B data pin 7	VDDQ_B0_B
DQ8_B	DIO	DRAM channel B data pin 8	VDDQ_B1_B
DQ9_B	DIO	DRAM channel B data pin 9	VDDQ_B1_B
DQ10_B	DIO	DRAM channel B data pin 10	VDDQ_B1_B
DQ11_B	DIO	DRAM channel B data pin 11	VDDQ_B1_B
DQ12_B	DIO	DRAM channel B data pin 12	VDDQ_B1_B
DQ13_B	DIO	DRAM channel B data pin 13	VDDQ_B1_B
DQ14_B	DIO	DRAM channel B data pin 14	VDDQ_B1_B
DQ15_B	DIO	DRAM channel B data pin 15	VDDQ_B1_B
DMI0_B	DIO	DRAM channel B DQM 0	VDDQ_B0_B
DMI1_B	DIO	DRAM channel B DQM 1	VDDQ_B1_B
DQS0_T_B	DIO	DRAM channel B DQS 0	VDDQ_B0_B
DQS0_C_B	DIO	DRAM channel B DQS 0 #	VDDQ_B0_B

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Pin name	Type	Description	Power domain
DQS1_T_B	DIO	DRAM channel B DQS 1	VDDQ_B1_B
DQS1_C_B	DIO	DRAM channel B DQS 1 #	VDDQ_B1_B
CA0_C	DIO	DRAM channel C address output 0	VDDQ_CA_C
CA1_C	DIO	DRAM channel C address output 1	VDDQ_CA_C
CA2_C	DIO	DRAM channel C address output 2	VDDQ_CA_C
CA3_C	DIO	DRAM channel C address output 3	VDDQ_CA_C
CA4_C	DIO	DRAM channel C address output 4	VDDQ_CA_C
CA5_C	DIO	DRAM channel C address output 5	VDDQ_CA_C
CKE0_C	DIO	DRAM channel C command output CKE 0	VDDQ_CA_C
CKE1_C	DIO	DRAM channel C command output CKE 1	VDDQ_CA_C
CK_T_C	DIO	DRAM channel C clock 0 output	VDDQ_CA_C
CK_C_C	DIO	DRAM channel C clock 0 output #	VDDQ_CA_C
CS0_C	DIO	DRAM channel C chip select 0 #	VDDQ_CA_C
CS1_C	DIO	DRAM channel C chip select 1 #	VDDQ_CA_C
DQ0_C	DIO	DRAM channel C data pin 0	VDDQ_C0_C
DQ1_C	DIO	DRAM channel C data pin 1	VDDQ_C0_C
DQ2_C	DIO	DRAM channel C data pin 2	VDDQ_C0_C
DQ3_C	DIO	DRAM channel C data pin 3	VDDQ_C0_C
DQ4_C	DIO	DRAM channel C data pin 4	VDDQ_C0_C
DQ5_C	DIO	DRAM channel C data pin 5	VDDQ_C0_C
DQ6_C	DIO	DRAM channel C data pin 6	VDDQ_C0_C
DQ7_C	DIO	DRAM channel C data pin 7	VDDQ_C0_C
DQ8_C	DIO	DRAM channel C data pin 8	VDDQ_C1_C
DQ9_C	DIO	DRAM channel C data pin 9	VDDQ_C1_C
DQ10_C	DIO	DRAM channel C data pin 10	VDDQ_C1_C
DQ11_C	DIO	DRAM channel C data pin 11	VDDQ_C1_C
DQ12_C	DIO	DRAM channel C data pin 12	VDDQ_C1_C
DQ13_C	DIO	DRAM channel C data pin 13	VDDQ_C1_C
DQ14_C	DIO	DRAM channel C data pin 14	VDDQ_C1_C
DQ15_C	DIO	DRAM channel C data pin 15	VDDQ_C1_C
DMI0_C	DIO	DRAM channel C DQM 0	VDDQ_C0_C
DMI1_C	DIO	DRAM channel C DQM 1	VDDQ_C1_C
DQS0_T_C	DIO	DRAM channel C DQS 0	VDDQ_C0_C
DQS0_C_C	DIO	DRAM channel C DQS 0 #	VDDQ_C0_C
DQS1_T_C	DIO	DRAM channel C DQS 1	VDDQ_C1_C
DQS1_C_C	DIO	DRAM channel C DQS 1 #	VDDQ_C1_C
CA0_D	DIO	DRAM channel D address output 0	VDDQ_DA_D
CA1_D	DIO	DRAM channel D address output 1	VDDQ_DA_D
CA2_D	DIO	DRAM channel D address output 2	VDDQ_DA_D
CA3_D	DIO	DRAM channel D address output 3	VDDQ_DA_D
CA4_D	DIO	DRAM channel D address output 4	VDDQ_DA_D
CA5_D	DIO	DRAM channel D address output 5	VDDQ_DA_D
CKE0_D	DIO	DRAM channel D command output CKE 0	VDDQ_DA_D

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Pin name	Type	Description	Power domain
CKE1_D	DIO	DRAM channel D command output CKE 1	VDDQ_DA_D
CK_T_D	DIO	DRAM channel D clock 0 output	VDDQ_DA_D
CK_D_D	DIO	DRAM channel D clock 0 output #	VDDQ_DA_D
CS0_D	DIO	DRAM channel D chip select 0 #	VDDQ_DA_D
CS1_D	DIO	DRAM channel D chip select 1 #	VDDQ_DA_D
DQ0_D	DIO	DRAM channel D data pin 0	VDDQ_D0_D
DQ1_D	DIO	DRAM channel D data pin 1	VDDQ_D0_D
DQ2_D	DIO	DRAM channel D data pin 2	VDDQ_D0_D
DQ3_D	DIO	DRAM channel D data pin 3	VDDQ_D0_D
DQ4_D	DIO	DRAM channel D data pin 4	VDDQ_D0_D
DQ5_D	DIO	DRAM channel D data pin 5	VDDQ_D0_D
DQ6_D	DIO	DRAM channel D data pin 6	VDDQ_D0_D
DQ7_D	DIO	DRAM channel D data pin 7	VDDQ_D0_D
DQ8_D	DIO	DRAM channel D data pin 8	VDDQ_D1_D
DQ9_D	DIO	DRAM channel D data pin 9	VDDQ_D1_D
DQ10_D	DIO	DRAM channel D data pin 10	VDDQ_D1_D
DQ11_D	DIO	DRAM channel D data pin 11	VDDQ_D1_D
DQ12_D	DIO	DRAM channel D data pin 12	VDDQ_D1_D
DQ13_D	DIO	DRAM channel D data pin 13	VDDQ_D1_D
DQ14_D	DIO	DRAM channel D data pin 14	VDDQ_D1_D
DQ15_D	DIO	DRAM channel D data pin 15	VDDQ_D1_D
DMI0_D	DIO	DRAM channel D DQM 0	VDDQ_D0_D
DMI1_D	DIO	DRAM channel D DQM 1	VDDQ_D1_D
DQS0_T_D	DIO	DRAM channel D DQS 0	VDDQ_D0_D
DQS0_D_D	DIO	DRAM channel D DQS 0 #	VDDQ_D0_D
DQS1_T_D	DIO	DRAM channel D DQS 1	VDDQ_D1_D
DQS1_D_D	DIO	DRAM channel D DQS 1 #	VDDQ_D1_D
RESET_N	DIO	DRAM RESET#	VDDQ_CA_B
Core Power			
DVDD_TOP	P	Digital power for core	-
DVDD_IPUSYS	P	Digital power for core	-
DVDD_SRAM_GPU	P	Digital power for core	-
DVDD_GPU	P	Digital power for core	-
DVDD_SRAM_TOP	P	Digital power for core	-
DVDD_SRAM_DVFS1	P	Digital power for core	-
DVDD_SRAM_DVFS2	P	Digital power for core	-
DVDD_SRAM_MODEM	P	Digital power for core	-
DVDD_MODEM	P	Digital power for core	-
DVDD_MD1	P	Digital power for core	-
PAD Power			
DVDD18_IOLT	P	Digital 1.8V power for IO	-
DVDD18_IOLB	P	Digital 1.8V power for IO	-
DVDD18_IOMC3	P	Digital 1.8V power for IO	-

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Pin name	Type	Description	Power domain
DVDD18_IOBL	P	Digital 1.8V power for IO	-
DVDD18_MSDC0	P	Digital 1.8V power for IO	-
DVDD18_IOBR	P	Digital 1.8V power for IO	-
DVDD28_MC2	P	Digital 3.0V power for IO	-
DVDD18_MC2	P	Digital 1.8V power for IO	-
DVDD28_SIM2	P	Digital 3.0V power for IO	-
DVDD28_SIM1	P	Digital 3.0V power for IO	-
DVDD28_MC1	P	Digital 3.0V power for IO	-
DVDD18_MC1	P	Digital 1.8V power for IO	-
DVDD18_IORB	P	Digital 1.8V power for IO	-
DVDD18_IOTR	P	Digital 1.8V power for IO	-
DVDD12_IOAUD	P	Digital 1.2V power for IO	-

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2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 2-4. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
DVDD_TOP	Digital power for core	0.585	0.88	V
DVDD_IPUSYS	Digital power for core	0.585	0.88	V
DVDD_SRAM_GPU	Digital power for core	0.72	1.0	V
DVDD_GPU	Digital power for core	0.511	1.0	V
DVDD_DVFS1	Digital power for core	0.511	1.03	V
DVDD_DVFS2	Digital power for core	0.511	1.03	V
DVDD_SRAM_TOP	Digital power for core	0.72	0.99	V
DVDD_SRAM_DVFS1	Digital power for core	0.72	1.03	V
DVDD_SRAM_DVFS2	Digital power for core	0.72	1.03	V
DVDD_SRAM_MODEM	Digital power for core	0.72	0.99	V
DVDD_MODEM	Digital power for core	0.585	0.88	V
DVDD_MD1	Digital power for core	0.585	0.77	V
DVDD18_EFUSE	EFUSE power	1.71	2.2	V
DVSS	Ground	0	0	V
DVDD18_IOLT	Digital 1.8V power for IO	1.62	1.98	V
DVDD18_IOLB	Digital 1.8V power for IO	1.62	1.98	V
DVDD18_IOMC3	Digital 1.8V power for IO	1.7	1.95	V
DVDD18_IOBL	Digital 1.8V power for IO	1.62	1.98	V
DVDD18_MSDC0	Digital 1.8V power for IO	1.7	1.95	V
DVDD18_IOBR	Digital 1.8V power for IO	1.62	1.98	V
DVDD28_MC2	Digital 3.0V power for IO	2.7	3.3	V
DVDD18_MC2	Digital 1.8V power for IO	1.7	1.95	V
DVDD28_SIM2	Digital 3.0V power for IO	2.7	3.3	V
DVDD28_SIM1	Digital 3.0V power for IO	2.7	3.3	V
DVDD18_SIM	Digital 1.8V power for IO	1.7	1.9	V
DVDD28_MC1	Digital 3.0V power for IO	2.7	3.3	V
DVDD18_MC1	Digital 1.8V power for IO	1.7	1.95	V
DVDD18_IORB	Digital 1.8V power for IO	1.62	1.98	V
DVDD18_IOTR	Digital 1.8V power for IO	1.62	1.98	V
DVDD12_IOAUD	Digital 1.2V power for IO	1.08	1.32	V
AVDD12_SSUSB	Analog power	1.08	1.32	V
AVDD09_SSUSB	Analog power	0.83	0.95	V
AVDD33_USB_P1	Analog power	2.76	3.35	V
AVDD12_USB_P1	Analog power	1.08	1.32	V
AVDD18_USB_P1	Analog power	1.62	1.98	V
AVDD33_USB_P0	Analog power	2.76	3.35	V
AVDD12_USB_P0	Analog power	1.08	1.32	V

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Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_USB_P0	Analog power	1.62	1.98	V
AVDD18_AP	Analog power	1.62	1.98	V
AVDD12_PLLGP	Analog power	1.08	1.32	V
AVDD09_PLLGP	Analog power	0.83	0.95	V
AVDD18_MD	Analog power	1.62	1.98	V
AVDD12_CSI	Analog power	1.08	1.32	V
AVDD18_CSI	Analog power	1.62	1.98	V
AVDD09_UFS	Analog power	0.83	0.95	V
AVDD12_UFS	Analog power	1.08	1.32	V
AVDD18_UFS	Analog power	1.62	1.98	V
AVDD04_DSI1	Analog power	0.585	0.88	V
AVDD12_DSI1	Analog power	1.08	1.32	V
AVDD18_DSI1	Analog power	1.62	1.98	V
AVDD04_DSI0	Analog power	0.585	0.88	V
AVDD12_DSI0	Analog power	1.08	1.32	V
AVDD18_DSI0	Analog power	1.62	1.98	V
VDDQ_CA_A	DRAM I/O power	1.06	1.17	V
VDDQ_B0_A	DRAM I/O power	1.06	1.17	V
VDDQ_B1_A	DRAM I/O power	1.06	1.17	V
VDD2_CA_A	DRAM I/O power	1.06	1.17	V
VDD2_B0_A	DRAM I/O power	1.06	1.17	V
VDD2_B1_A	DRAM I/O power	1.06	1.17	V
AVDD12_A	Analog power	1.2	1.2	V
VDDQ_CA_B	DRAM I/O power	1.06	1.17	V
VDDQ_B0_B	DRAM I/O power	1.06	1.17	V
VDDQ_B1_B	DRAM I/O power	1.06	1.17	V
VDD2_CA_B	DRAM I/O power	1.06	1.17	V
VDD2_B0_B	DRAM I/O power	1.06	1.17	V
VDD2_B1_B	DRAM I/O power	1.06	1.17	V
AVDD12_B	Analog power	1.2	1.2	V
VDDQ_CA_C	DRAM I/O power	1.06	1.17	V
VDDQ_B0_C	DRAM I/O power	1.06	1.17	V
VDDQ_B1_C	DRAM I/O power	1.06	1.17	V
VDD2_CA_C	DRAM I/O power	1.06	1.17	V
VDD2_B0_C	DRAM I/O power	1.06	1.17	V
VDD2_B1_C	DRAM I/O power	1.06	1.17	V
AVDD12_C	Analog power	1.2	1.2	V
VDDQ_CA_D	DRAM I/O power	1.06	1.17	V
VDDQ_B0_D	DRAM I/O power	1.06	1.17	V
VDDQ_B1_D	DRAM I/O power	1.06	1.17	V
VDD2_CA_D	DRAM I/O power	1.06	1.17	V
VDD2_B0_D	DRAM I/O power	1.06	1.17	V
VDD2_B1_D	DRAM I/O power	1.06	1.17	V

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Symbol or pin name	Description	Min.	Max.	Unit
AVDD12_D	Analog power	1.2	1.2	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-5. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD_TOP	Digital power for core	0.585	0.8	0.88	V
DVDD_IPUSYS	Digital power for core	0.585	0.8	0.88	V
DVDD_SRAM_GPU	Digital power for core	0.72	0.973	1.0	V
DVDD_GPU	Digital power for core	0.511	0.973	1.0	V
DVDD_DVFS1	Digital power for core	0.511	1.0	1.03	V
DVDD_DVFS2	Digital power for core	0.511	1.0	1.03	V
DVDD_SRAM_TOP	Digital power for core	0.72	0.9	0.99	V
DVDD_SRAM_DVFS1	Digital power for core	0.72	1.0	1.03	V
DVDD_SRAM_DVFS2	Digital power for core	0.72	1.0	1.03	V
DVDD_SRAM_MODEM	Digital power for core	0.72	0.9	0.99	V
DVDD_MODEM	Digital power for core	0.585	0.8	0.88	V
DVDD_MD1	Digital power for core	0.585	0.7	0.77	V
DVDD18_EFUSE	EFUSE power	1.71	2	2.2	V
DVSS	Ground	0	0	0	V
DVDD18_IOLT	Digital 1.8V power for IO	1.7	1.8	1.98	V
DVDD18_IOLB	Digital 1.8V power for IO	1.7	1.8	1.98	V
DVDD18_IOMC3	Digital 1.8V power for IO	1.7	1.8	1.95	V
DVDD18_IOBL	Digital 1.8V power for IO	1.7	1.8	1.98	V
DVDD18_MSDC0	Digital 1.8V power for IO	1.7	1.8	1.95	V
DVDD18_IOBR	Digital 1.8V power for IO	1.7	1.8	1.98	V
DVDD18_MC2	Digital 1.8V power for IO	1.7	1.8	1.95	V
DVDD18_SIM	Digital 1.8V power for IO	1.7	1.8	1.9	V
DVDD18_MC1	Digital 1.8V power for IO	1.7	1.8	1.95	V
DVDD18_IORB	Digital 1.8V power for IO	1.7	1.8	1.9	V
DVDD18_IOTR	Digital 1.8V power for IO	1.7	1.8	1.98	V
DVDD12_IOAUD	Digital 1.2V power for IO	1.08	1.2	1.32	V
DVDD28_MC1	Digital 3.0V power input for MSDC1	2.7	3	3.3	V
		1.7	1.8	1.9	
DVDD28_MC2	Digital 3.0V power input for MSDC2	2.7	3	3.3	V
		1.7	1.8	1.9	
DVDD28_SIM1	Digital 3.0V power input for SIM1	2.7	3	3.3	V
		1.7	1.8	1.9	
DVDD28_SIM2	Digital 3.0V power input for SIM2	2.7	3	3.3	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
		1.7	1.8	1.9	
DVDD12_IOAUD	Digital 1.2V power input for Audio	1.08	1.2	1.32	V
		1.7	1.8	1.9	
AVDD12_SSUSB	Analog power	1.14	1.2	1.26	V
AVDD09_SSUSB	Analog power	0.84	0.875	0.915	V
AVDD33_USB_P1	Analog power	2.92	3.07	3.22	V
AVDD12_USB_P1	Analog power	1.14	1.2	1.26	V
AVDD18_USB_P1	Analog power	1.7	1.8	1.9	V
AVDD33_USB_P0	Analog power	2.92	3.07	3.22	V
AVDD12_USB_P0	Analog power	1.14	1.2	1.26	V
AVDD18_USB_P0	Analog power	1.7	1.8	1.9	V
AVDD18_AP	Analog power	1.7	1.8	1.9	V
AVDD12_PLLGP	Analog power	1.14	1.2	1.26	V
AVDD09_PLLGP	Analog power	0.84	0.875	0.915	V
AVDD18_MD	Analog power	1.7	1.8	1.9	V
AVDD12_CSI	Analog power	1.14	1.2	1.26	V
AVDD18_CSI	Analog power	1.7	1.8	1.9	V
AVDD09_UFS	Analog power	0.84	0.875	0.915	V
AVDD12_UFS	Analog power	1.14	1.2	1.26	V
AVDD18_UFS	Analog power	1.7	1.8	1.9	V
AVDD04_DSI1	Analog power	0.57	0.6	0.88	V
AVDD12_DSI1	Analog power	1.14	1.2	1.26	V
AVDD18_DSI1	Analog power	1.7	1.8	1.9	V
AVDD04_DSI0	Analog power	0.57	0.6	0.88	V
AVDD12_DSI0	Analog power	1.14	1.2	1.26	V
AVDD18_DSI0	Analog power	1.7	1.8	1.9	V
DDRV_D	DRAM I/O power	1.14	1.2	1.3	V
DDRV_D	DRAM I/O power	1.14	1.2	1.3	V
DDRVPOP	DRAM I/O power	1.14	1.2	1.3	V
VBIASN1_D	DRAM VBIASN power	0.2	0.2	0.2	V
VBIASN1_D	DRAM VBIASN power	0.2	0.2	0.2	V
VBIASNPOP	DRAM VBIASN power	0.2	0.2	0.2	V
VDD1	DRAM VDD1 core power	1.7	1.8	1.95	V
VDDQ	DRAM I/O power	1.14	1.2	1.3	V
VREF(CA)_D	DRAM VREF (CA) power	0.588	0.6	0.612	V
VREF(CA)_D	DRAM VREF (CA) power	0.588	0.6	0.612	V
VREF(DQ)_D	DRAM VREF (DQ) power	0.588	0.6	0.612	V
VREF(DQ)_D	DRAM VREF (DQ) power	0.588	0.6	0.612	V
VREF_D	DRAM VREF power	0.588	0.6	0.612	V
VREF_D	DRAM VREF power	0.588	0.6	0.612	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subject to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory conditions of ≤ 30°C/60% RH, or
   - Stored at ≤ 20% RH.
3. Devices require baking before mounting, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C for high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 I2C4/6/7, RTC, DPI DC Electrical Characteristics

Table 2-6. I2C4, I2C6, I2C7, RTC, DPI DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC output logic high voltage			0.25*DVDD18_IORB	V
F_{RTC}	Input clock frequency		32		KHz
DC_{RTC}	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI0/1/2, I2S1/2, I2C1/2, UART0/1/2 DC Electrical Characteristics

Table 2-7. SPI0, SPI1, SPI2, I2S1, I2S2, I2C0, I2C1, I2C2, UART0, UART1, UART2 DC electrical characteristics (DVDD18_IOBR =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOBR		DVDD18_IOBR + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOBR	V
VOH	DC output logic low voltage	0.75*DVDD18_IOBR			V
VOL	DC Output logic high voltage			0.25*DVDD18_IOBR	V

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2.2.4.3 UART3, I2C3 DC Electrical Characteristics

Table 2-8. UART3, I2C3 DC electrical characteristics (DVDD18_IOBL =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOBL		DVDD18_IOBL + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOBL	V
VOH	DC output logic low voltage	0.75*DVDD18_IOBL			V
VOL	DC output logic high voltage			0.25*DVDD18_IOBL	V

2.2.4.4 SPI3, I2C5, BPI, BSI DC Electrical Characteristics

Table 2-9. SPI3, I2C5, BPI, BSI DC electrical characteristics (DVDD18_IOTR =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOTR		DVDD18_IOTR + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOTR	V
VOH	DC output logic low voltage	0.75*DVDD18_IOTR			V
VOL	DC output logic high voltage			0.25*DVDD18_IOTR	V

2.2.4.5 BPI, BSI DC Electrical Characteristics

Table 2-10. BPI, BSI electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V

2.2.4.6 JTAG DC Electrical Characteristics

Table 2-11. JTAG DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLB			V

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Parameters	Descriptions	Min.	Typ.	Max.	Unit
VOL	DC output logic high voltage			0.25*DVDD18_IOLB	V

2.2.4.7 MSDC0 DC Electrical Characteristics

Table 2-12. MSDC0 DC electrical characteristics (DVDD18_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.27		DVDD18_MSDC0 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD18_MSDC0 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.8 MSDC1 DC Electrical Characteristics

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MC1=3.0V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625* DVDD28_MC1		DVDD28_MC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MC1		DVDD28_MC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MC1	V

Table 2-14. MSDC1 DC electrical characteristics (DVDD18_MC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD18_MC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD18_MC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

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2.2.4.9 MSDC3 DC Electrical Characteristics

Table 2-15. MSDC3 DC electrical characteristics (DVDD18_IOMC3=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.27		DVDD18_IOMC3 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD18_IOMC3 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.10 SIM DC Electrical Characteristics

Table 2-16. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

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2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR4/LPDDR4X

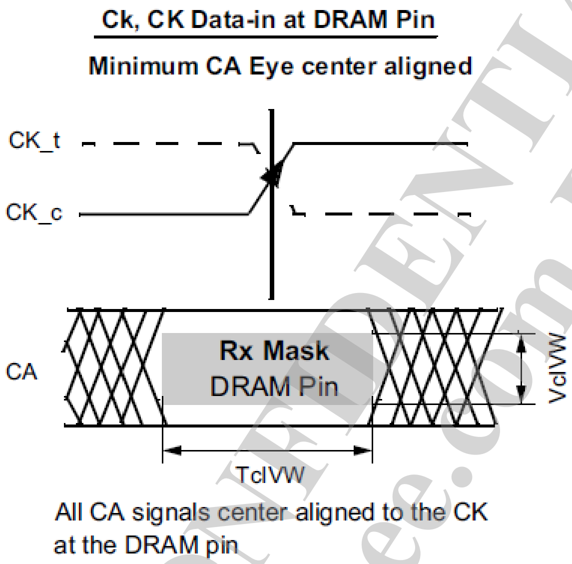

Figure 2-3. Basic timing parameter for LPDDR4 commands

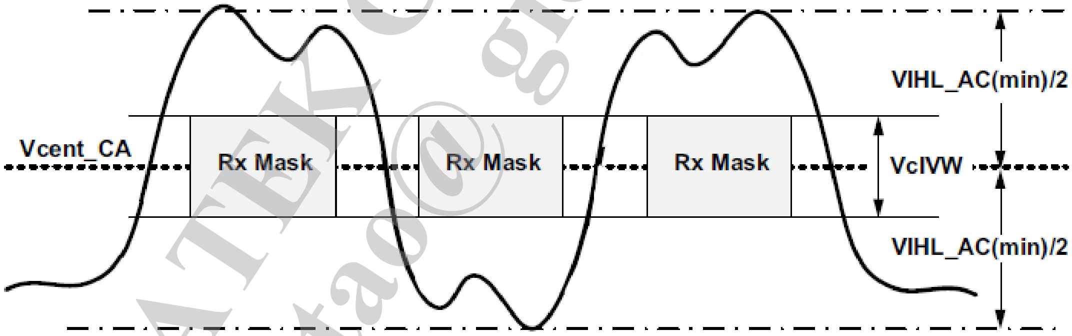

Figure 2-4. CA VIHL_AC definition for LPDDR4 commands

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Table 2-17. CA VIHL_AC definition for LPDDR4 commands

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit
		min	max	min	max	min	max	min	max	
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns

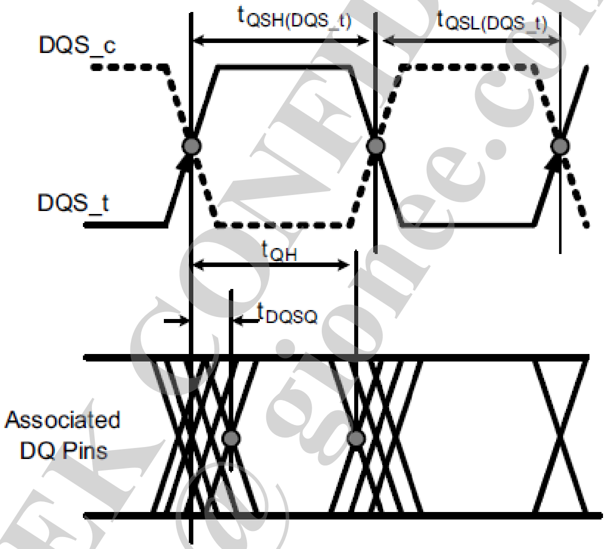

Figure 2-5. LPDDR4 read data timing

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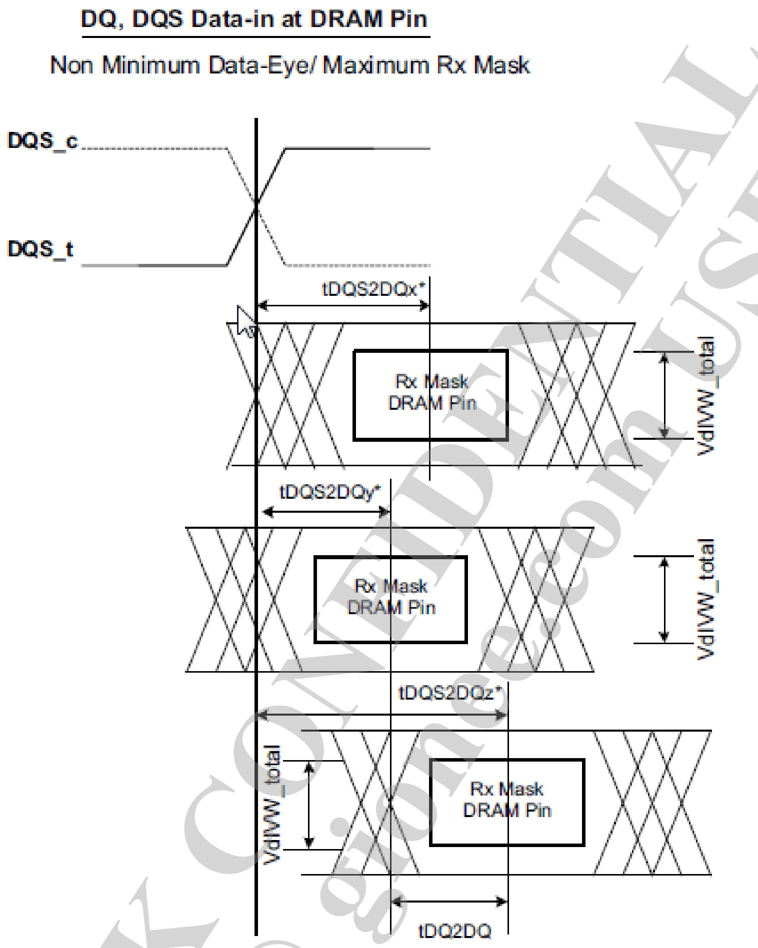

Figure 2-6. LPDDR4 write data timing

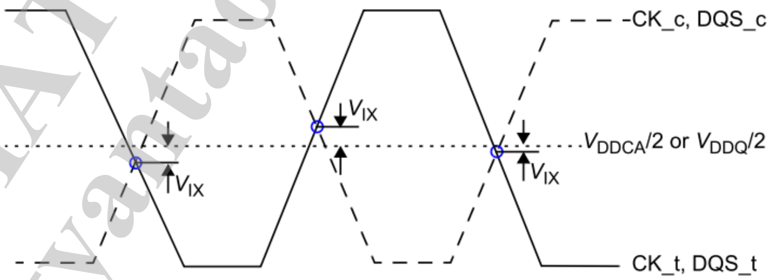

Figure 2-7. LPDDR4/LPDDR4X VIX definition

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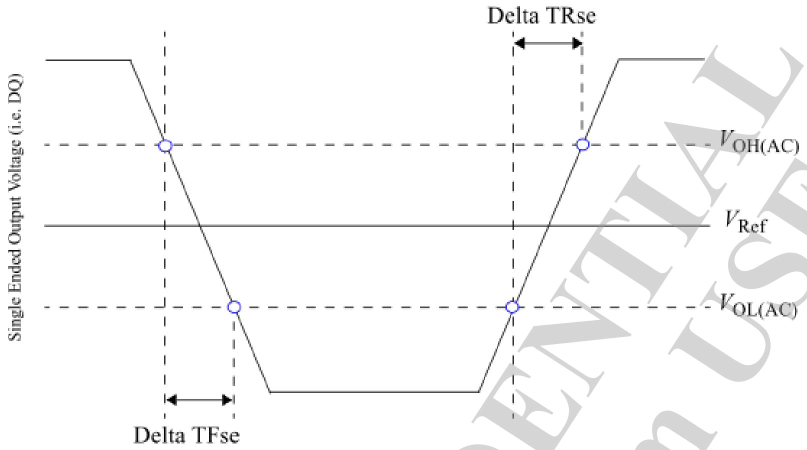

Figure 2-8. LPDDR4/LPDDR4X single-ended output slew-rate definition

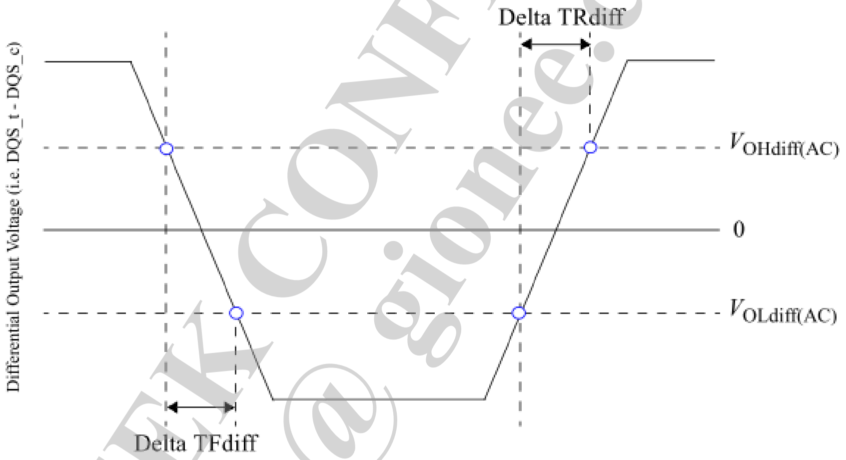

Figure 2-9. LPDDR4/LPDDR4X differential output slew-rate definition

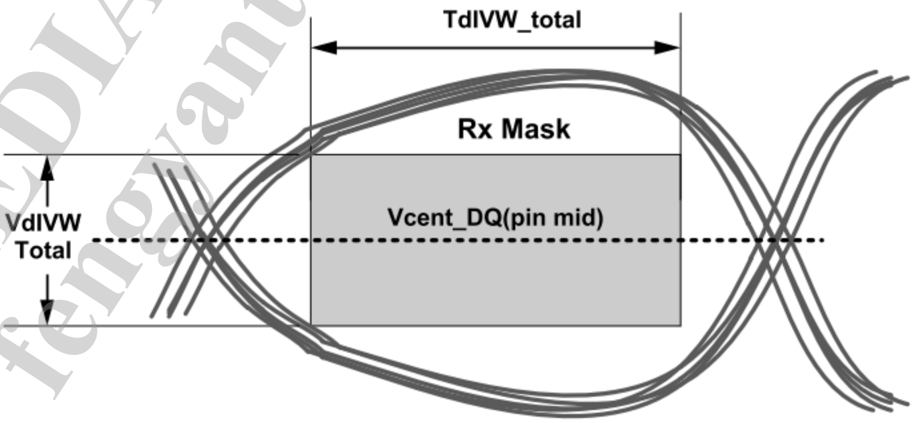

Figure 2-10. LPDDR4/LPDDR4X RX mask

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Table 2-18. LPDDR4/LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK Differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4)	Single-ended Output Slew Rate	3.5		9	V/ns
SRQse (LPDDR4X)	Single-ended Output Slew Rate	3		9	V/ns
SRQdiff (LPDDR4)	Differential Output Slew Rate	7		18	V/ns
SRQdiff (LPDDR4X)	Differential Output Slew Rate	6		18	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (At VdIVW voltage levels)			0.25	UI

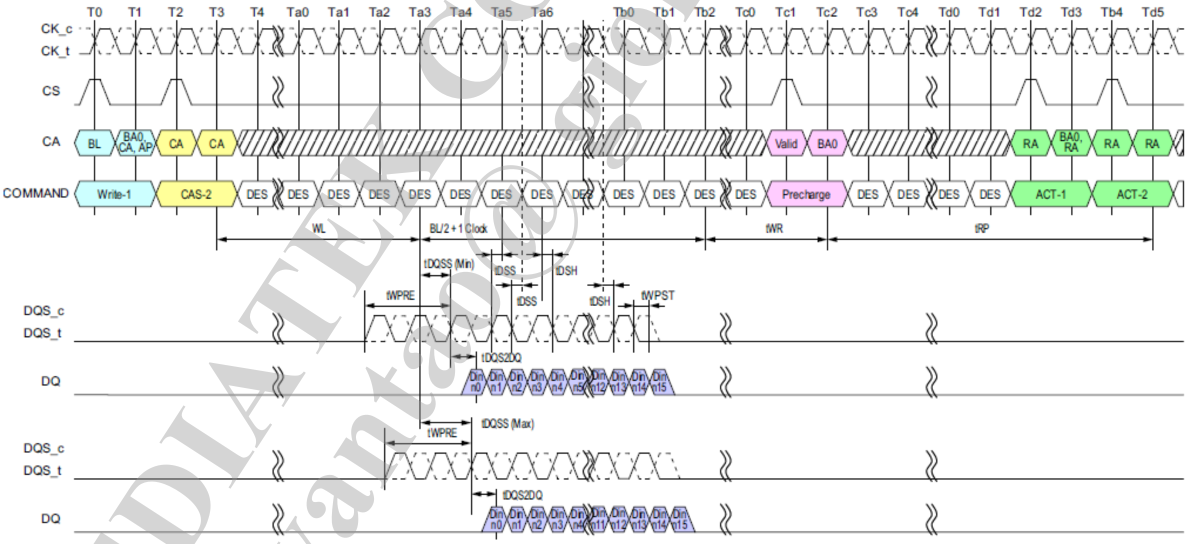

Figure 2-11. LPDDR4/LPDDR4X burst write operation

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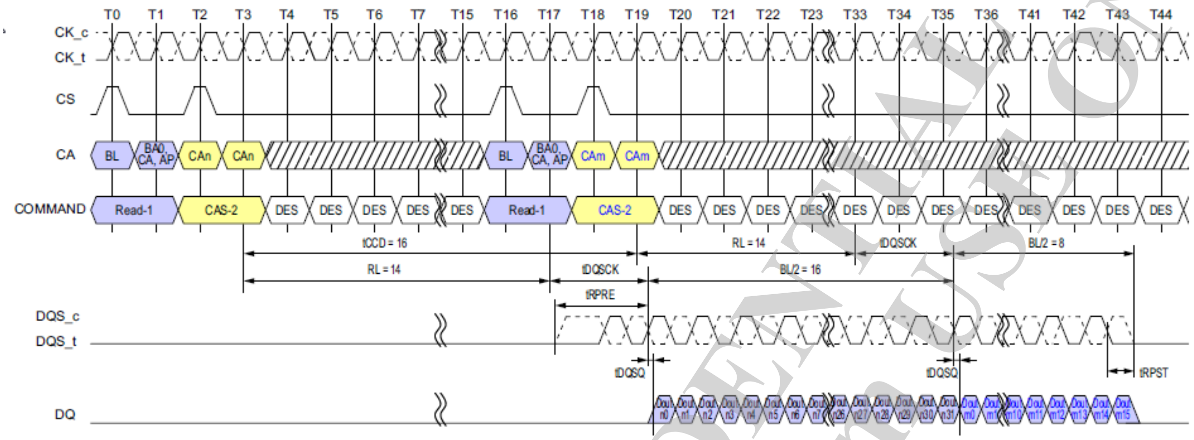

Figure 2-12. LPDDR4/LPDDR4X burst read operation

Table 2-19. LPDDR4/LPDDR4X clock AC timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200	
		Min	Max	Min	Max	Min	Max
Clock Timing							
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80

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Table 2-20. LPDDR4/LPDDR4X AC timing parameter table of external memory interface

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min/Max</th><th colspan="8">Data Rate</th><th rowspan="2">Unit</th></tr>
<tr><th colspan="3">Core Parameters</th><th>533</th><th>1066</th><th>1600</th><th>2133</th><th>2667</th><th>3200</th><th>3733</th><th>4267</th></tr>
<tr><td>ACTIVATE-to-ACTIVATE command period (same bank)</td><td>tRC</td><td>MIN</td><td colspan="8">tRAS + tRPab (with all-bank precharge)
tRAS + tRPpb (with per-bank precharge)</td><td>ns</td></tr>
<tr><td>Minimum Self-Refresh Time (Entry to Exit)</td><td>tSR</td><td>MIN</td><td colspan="8">max(15ns, 3nCK)</td><td>ns</td></tr>
<tr><td>SELF REFRESH exit to next valid command delay</td><td>tXSR</td><td>MIN</td><td colspan="8">max(tRFCab + 7.5ns, 2nCK)</td><td>ns</td></tr>
<tr><td>Exit Power-Down to next valid command delay</td><td>tXP</td><td>MIN</td><td colspan="8">max(7.5ns, 3nCK)</td><td>ns</td></tr>
<tr><td>CAS-to-CAS delay</td><td>tCCD</td><td>MIN</td><td colspan="8">8</td><td>tCK(avg)</td></tr>
<tr><td>Internal READ to PRECHARGE command delay</td><td>tRTP</td><td>MIN</td><td colspan="8">max(7.5ns, 8nCK)</td><td>ns</td></tr>
<tr><td>RAS-to-CAS delay</td><td>tRCD</td><td>MIN</td><td colspan="8">max(18ns, 4nCK)</td><td>ns</td></tr>
<tr><td>Row precharge time (single bank)</td><td>tRPpb</td><td>MIN</td><td colspan="8">max(18ns, 3nCK)</td><td>ns</td></tr>
<tr><td>Row precharge time (all banks)</td><td>tRPab</td><td>MIN</td><td colspan="8">max(21ns, 3nCK)</td><td>ns</td></tr>
<tr><td rowspan="2">Row active time</td><td rowspan="2">tRAS</td><td>MIN</td><td colspan="8">max(42ns, 3nCK)</td><td>ns</td></tr>
<tr><td>MAX</td><td colspan="8">Min(9 * tREFI * Refresh Rate, 70.2) us
(Refresh Rate is specified by MR4, OP[2:0])</td><td>-</td></tr>
<tr><td>WRITE recovery time</td><td>tWR</td><td>MIN</td><td colspan="8">max(18ns, 4nCK)</td><td>ns</td></tr>
<tr><td>WRITE-to-READ delay</td><td>tWTR</td><td>MIN</td><td colspan="8">max(10ns, 8nCK)</td><td>ns</td></tr>
<tr><td>Active bank-A to active bank-B</td><td>tRRD</td><td>MIN</td><td colspan="8">max(10ns, 4nCK)</td><td>ns</td></tr>
<tr><td>Precharge to Precharge Delay[1]</td><td>tPPD</td><td>MIN</td><td colspan="8">4</td><td>tCK</td></tr>
<tr><td>Four-bank ACTIVATE window</td><td>tFAW</td><td>MIN</td><td colspan="8">40</td><td>ns</td></tr>
</table>

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2.2.5.2 SPI AC Timing Characteristics

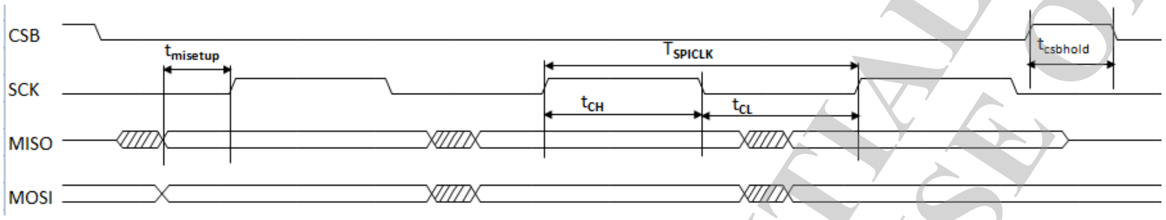

Figure 2-13. SPI timing diagram

Table 2-21. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

2.2.5.3 I2S AC Timing Characteristics

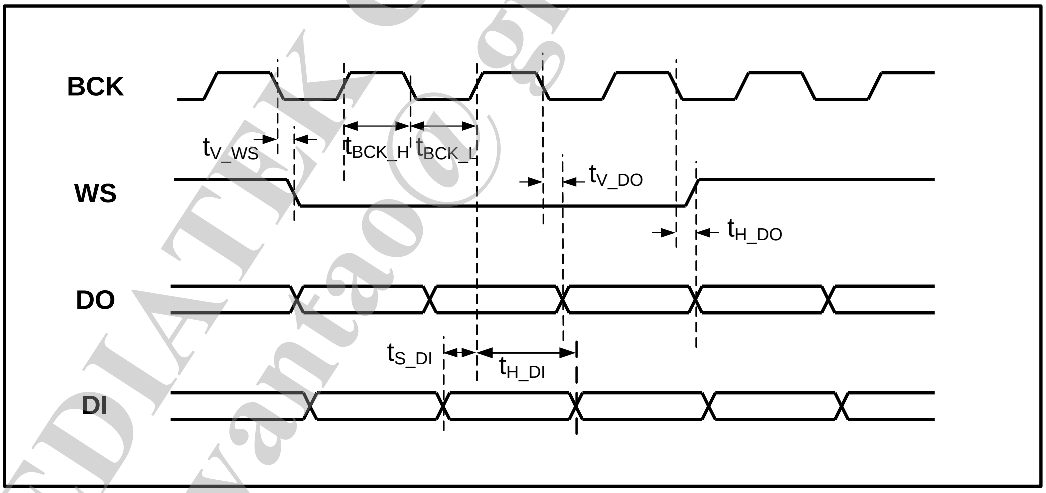

Figure 2-14. I2S master mode timing diagram

Table 2-22. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz

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Parameter	Description	Min.	Typ.	Max.	Unit
f_{BCK}	Serial clock frequency	32 * fs	-	64 * fs	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

2.2.5.4 I2C AC Timing Characteristics

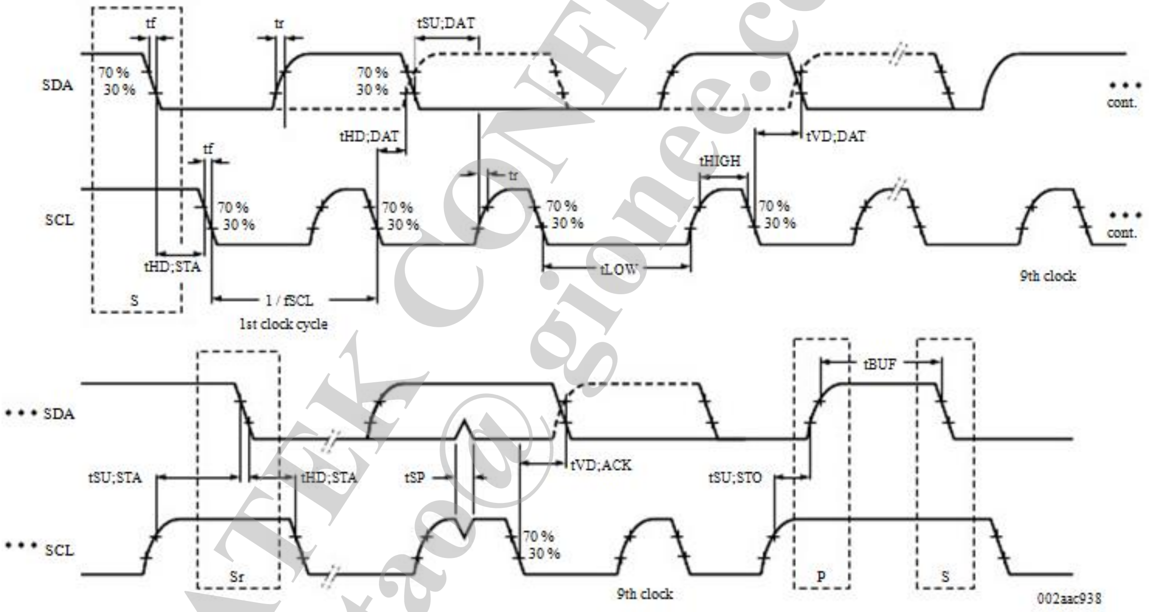

Figure 2-15. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-23. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	

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Symbol	Standard mode	Fast mode	Unit	Note
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

2.2.5.5 MSDC AC Timing Characteristics

2.2.5.5.1 Default Speed Timing

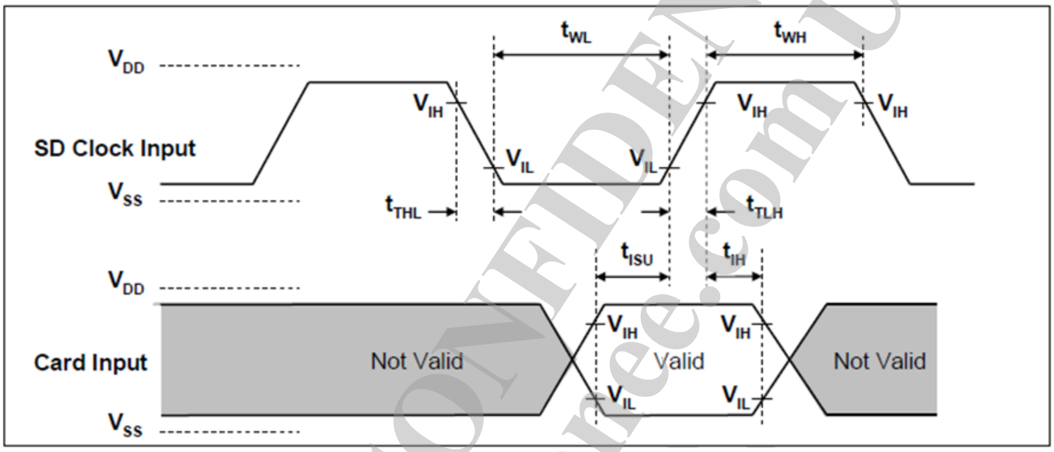

Figure 2-16. MSDC input timing diagram of default speed

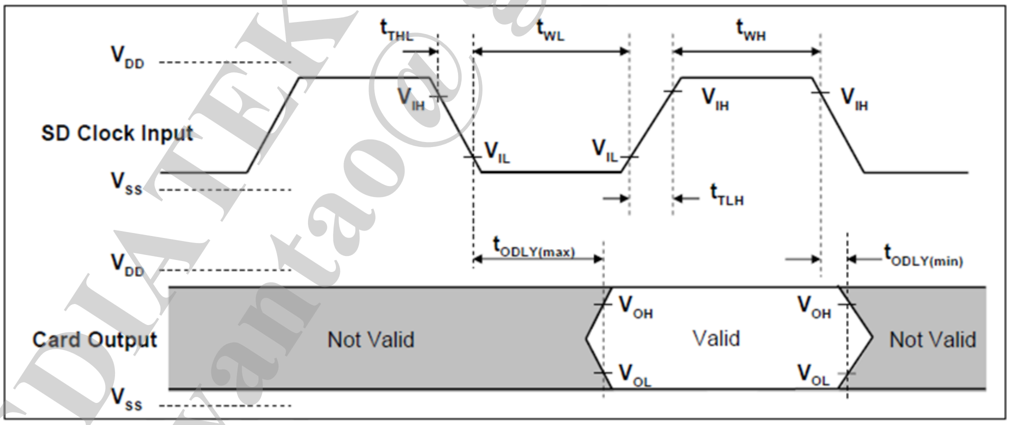

Figure 2-17. MSDC output timing diagram of default speed

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Table 2-24. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0(1) / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.5.2 High Speed Timing

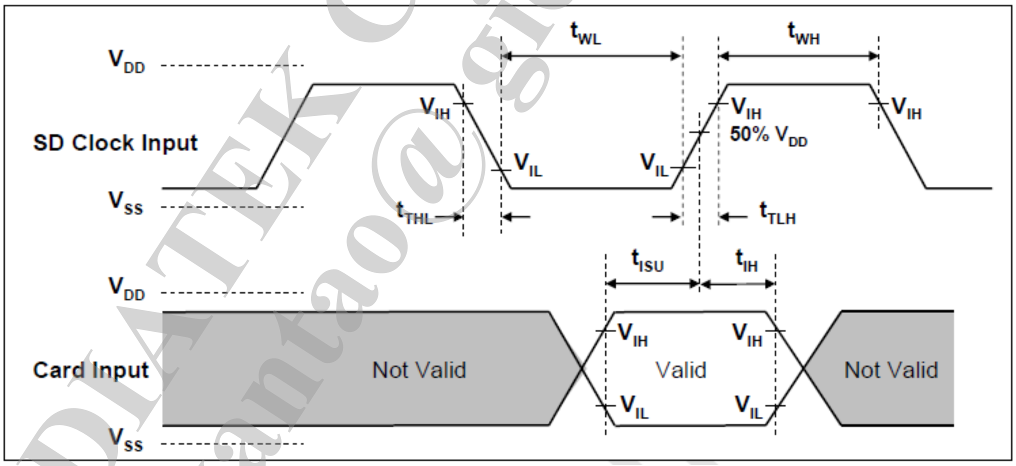

Figure 2-18. MSDC input timing diagram of high speed

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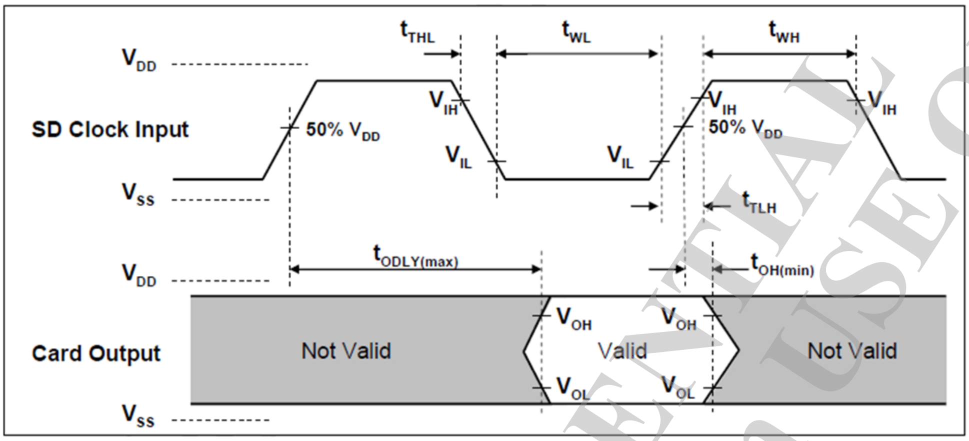

Figure 2-19. MSDC output timing diagram of high speed

Table 2-25. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L≦40pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L≧15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.5.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

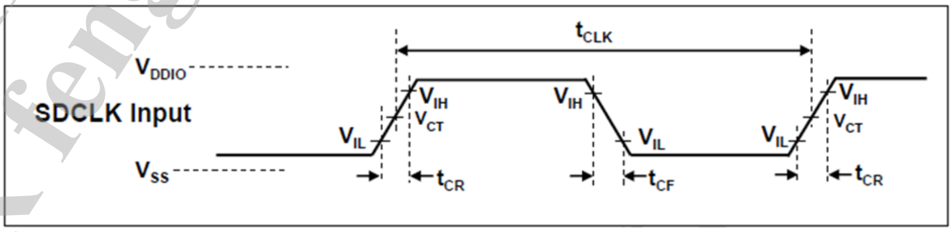

Figure 2-20. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

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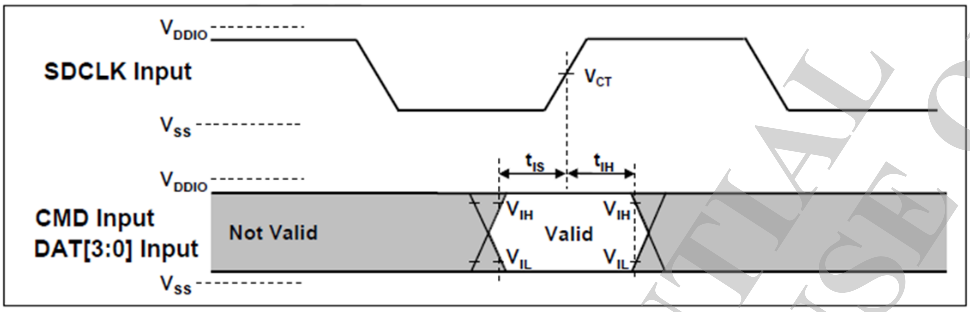

Figure 2-21. MSDC input timing diagram of SDR50/SDR104 mode

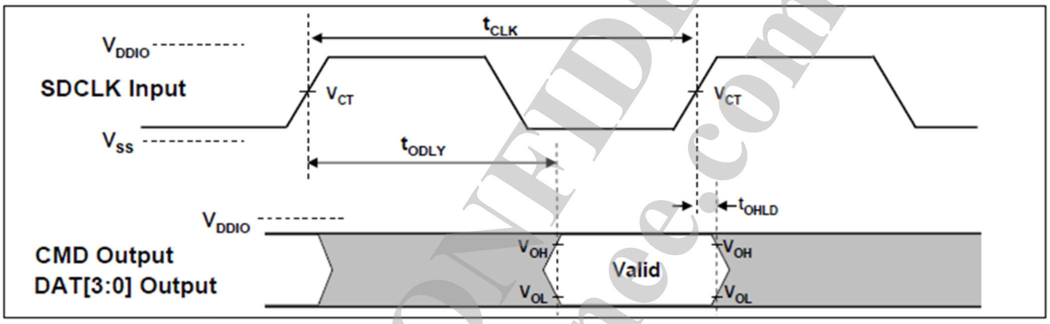

Figure 2-22. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

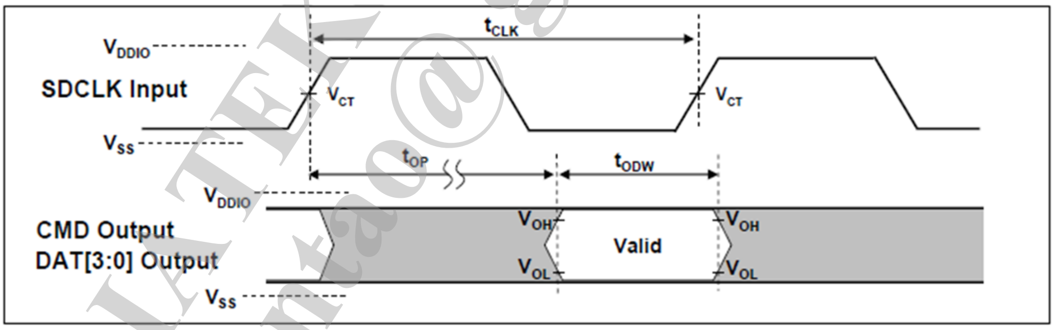

Figure 2-23. MSDC output timing diagram of variable window (SDR104)

Table 2-26. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.

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Symbol	Min.	Max.	Unit	Remark
Clock Duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.5.4 DDR50 Speed Mode Timing

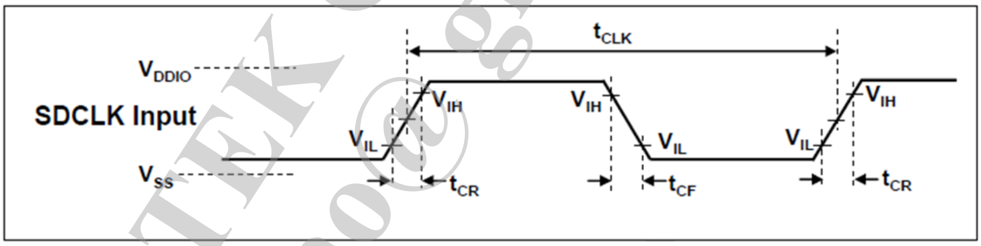

Figure 2-24. MSDC clock timing diagram of DDR50 speed mode

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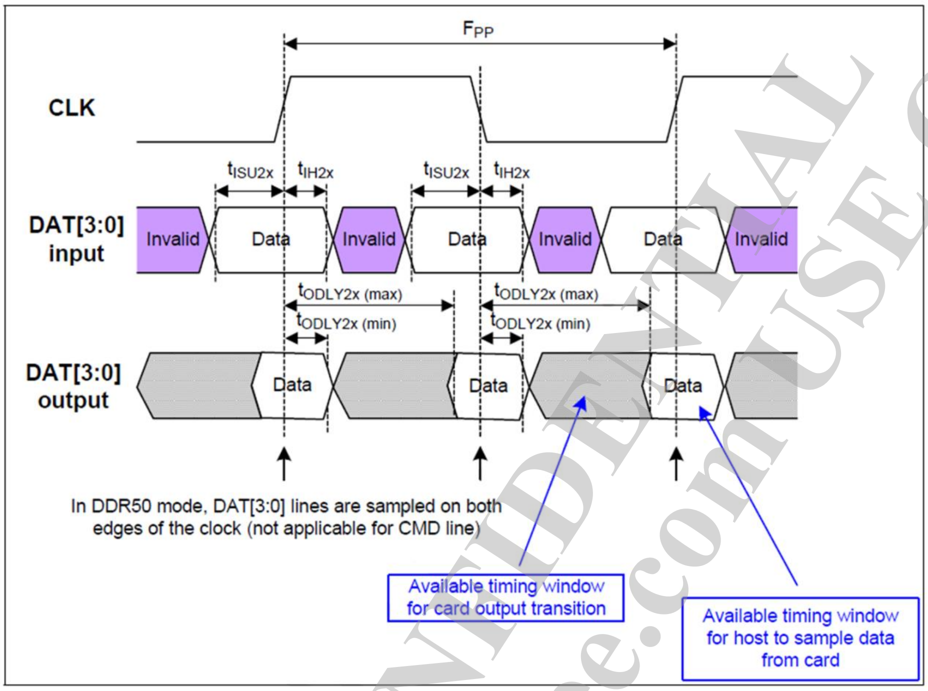

Figure 2-25. MSDC input/output timing diagram of DDR50 speed mode

Table 2-27. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

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2.2.5.5.5 HS200 Speed Timing

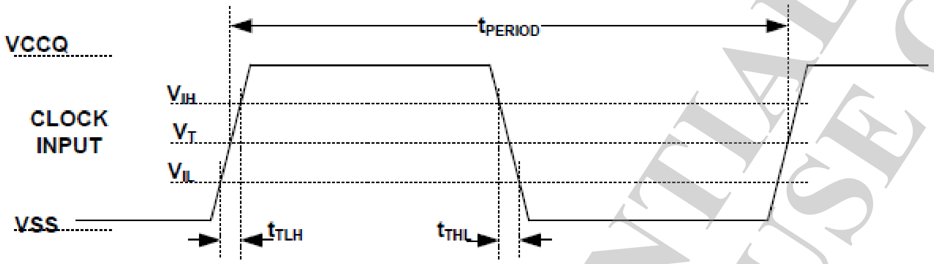
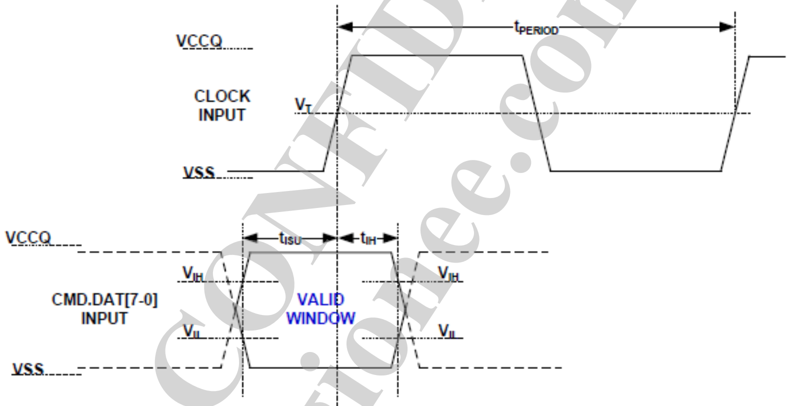


Figure 2-26. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-27. MSDC input timing diagram of HS200

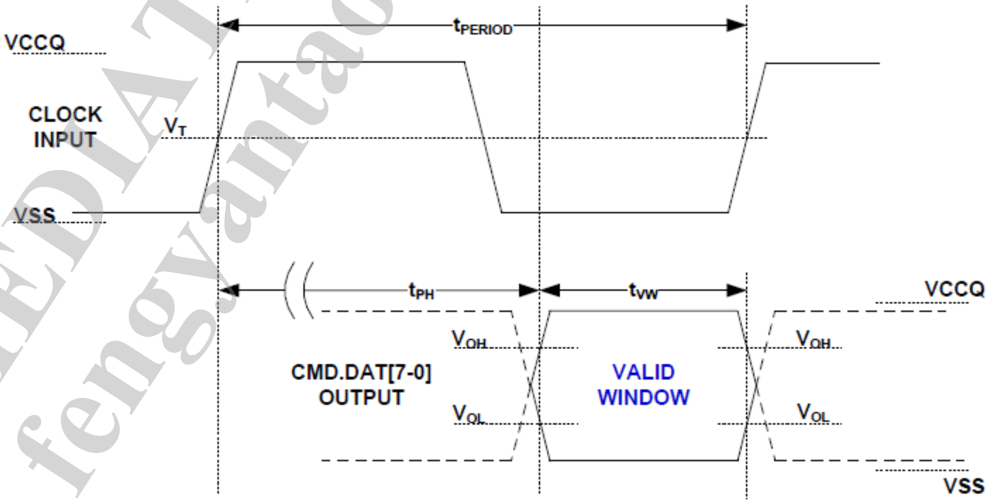


Figure 2-28. MSDC output timing diagram of HS200

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Table 2-28. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (Max), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	C_{DEVICE}≦6pF
t_{IH}	0.80		ns	C_{DEVICE}≦6pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay varioation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.5.6 HS400 Speed Timing

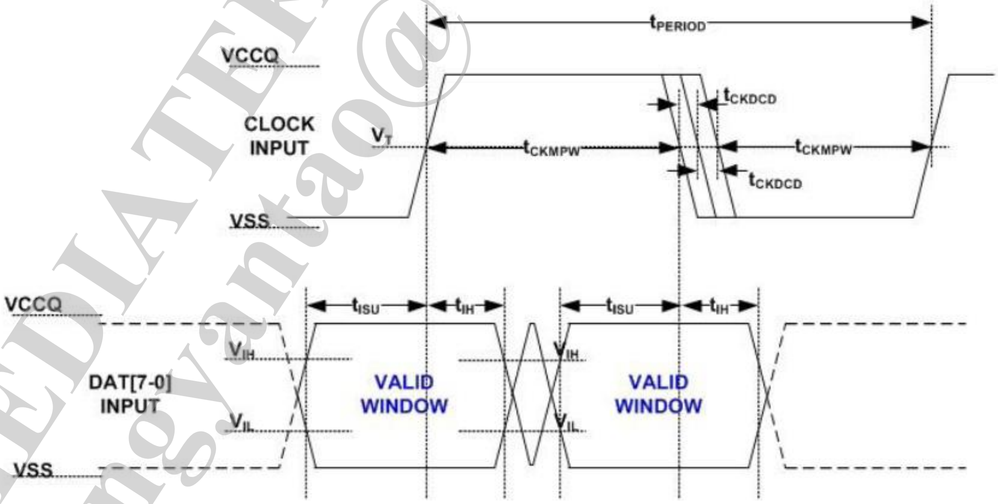

Figure 2-29. MSDC input timing diagram of HS400

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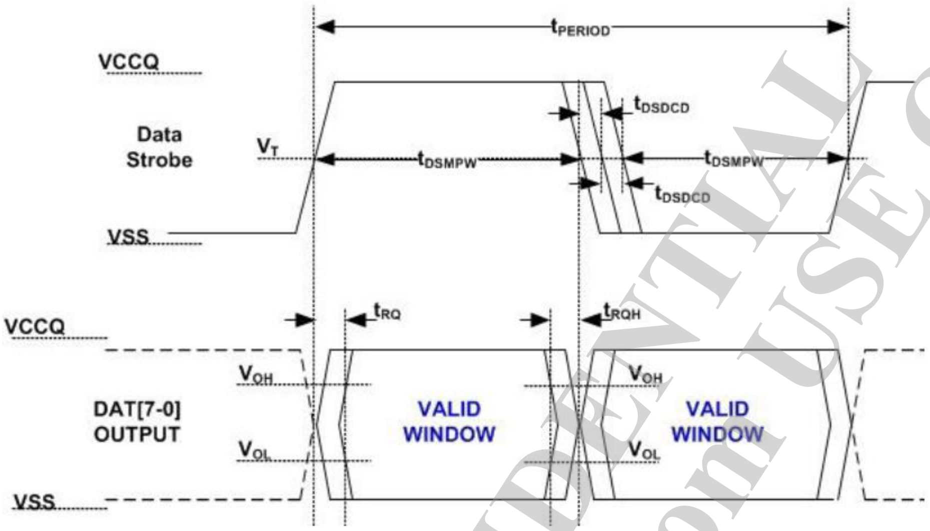

Figure 2-30. MSDC output timing diagram of HS400

Table 2-29. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leqq$ 6pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leqq$ 6pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.

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Parameter	Symbol	Min.	Max.	Unit	Remark
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.6 SIM AC Timing Characteristics

Table 2-30. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-31. Mode selection of chip

Pin name	Description
KPCOL0	0: Trigger USB download without battery 1: NA
KPROW0	0: Trigger USB download without battery 1: NA

2.3.2 Constant Tied Pins

Table 2-32. Constant tied pins of chip

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

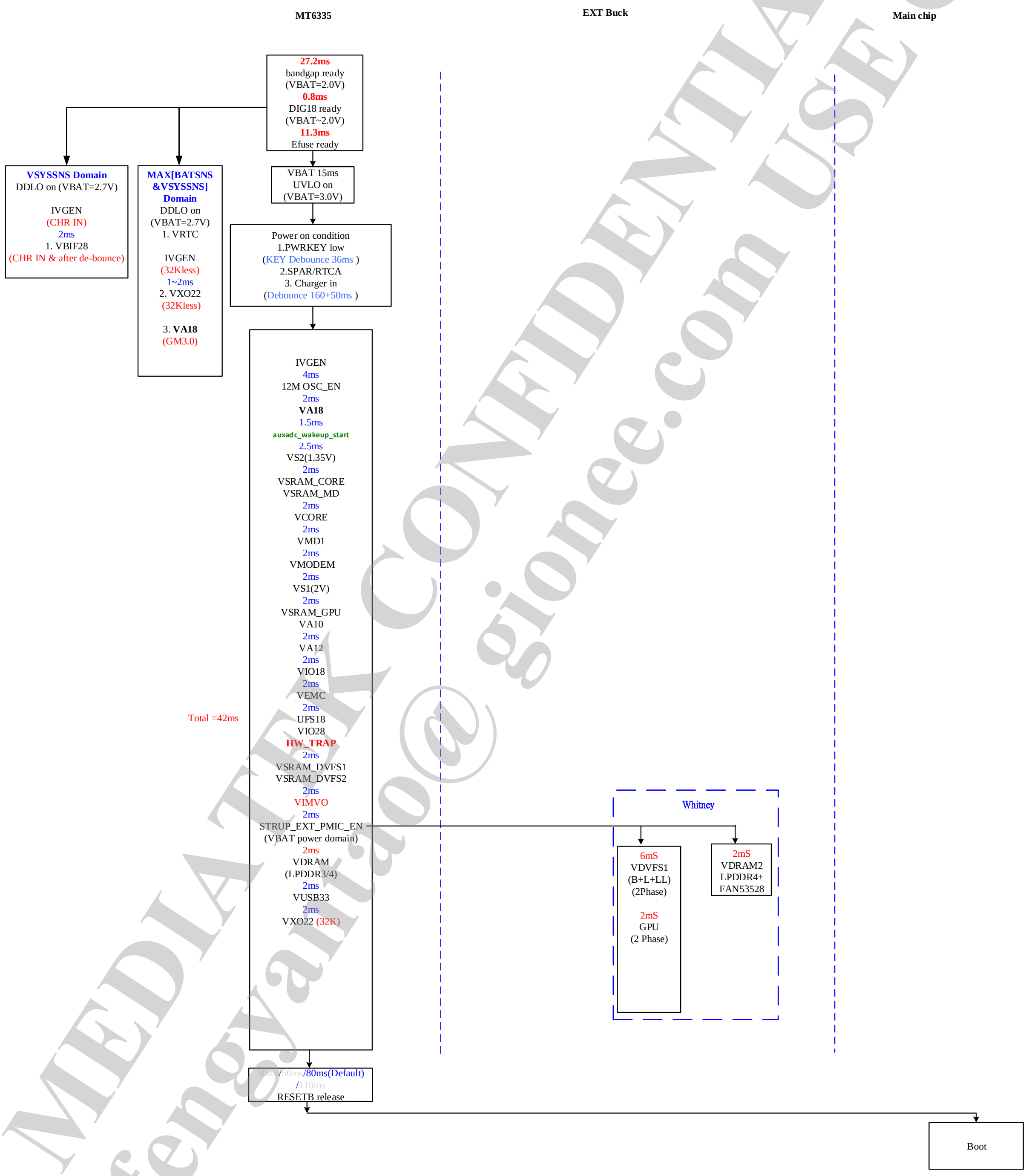

Figure 2-31. Power on/off sequence with XTAL

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: DAC output to control buck-converter for envelop tracking technique.
- RF control: DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers respectively.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

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A/D converter: 16 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

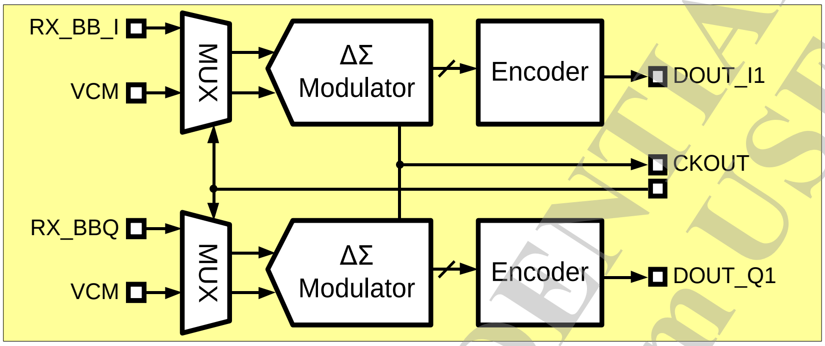

Figure 2-32. Block diagram of BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-33. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
RIN	Differential input resistance	2.8		20.8	kΩ
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	−20		80	°C

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

Each BBTX includes two channel DACs with the 1st order low pass filter.

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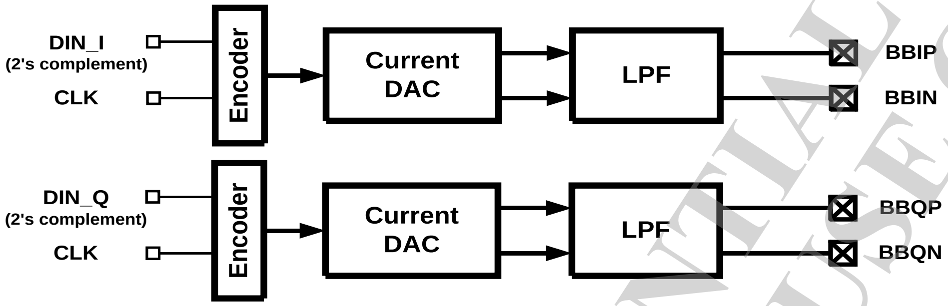

Figure 2-33. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-34. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	-20		80	°C

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. D/A converter: Converts digital modulated signals to analog domain.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 1st-order filter frequency response.

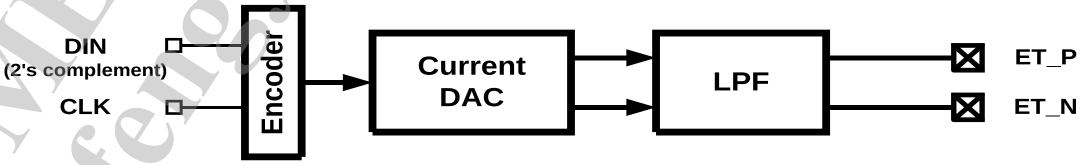

Figure 2-34. Block diagram of ETDAC

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2.5.3.3.2 Functional Specfications

Table 2-35. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	-20		80	°C

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.
2. A/D converters: Convert the detected signals to digital data.

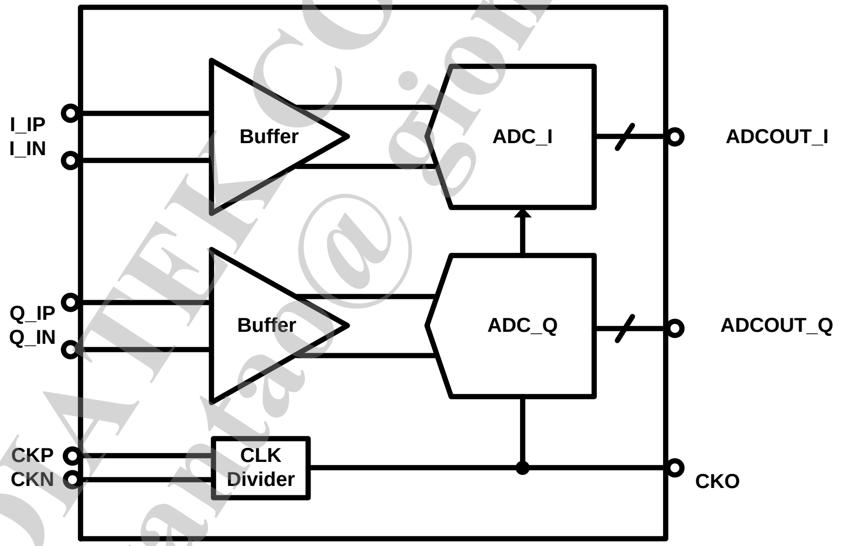

Figure 2-35. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

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Table 2-36. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	−20		80	°C

2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

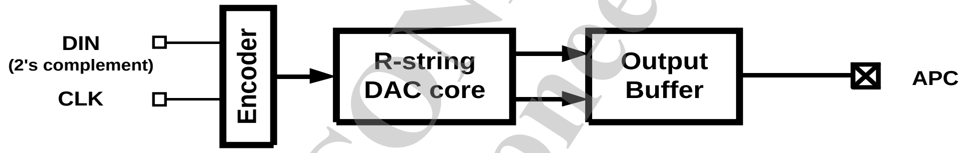

Figure 2-36. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-37. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Clock rate	1.0833		2.1666	MS/s
TS	Settling time (99% full-swing settling)			5	us
VO, max	Maximum output			AVDD – 0.2	V
CL	Output loading capacitance		220	2200	pF
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	−20		85	°C

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2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

Table 2-38. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	External use (AUX_IN2)
Channel 3	External use (AUX_IN3)
Channel 4	External use (AUX_IN4)
Channel 5~15	NA

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-39. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		3.25/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance		5		pF
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

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2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-40. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Vin	Input signal amplitude	400	800	1,200	mVpp
	Maximum positive overshoot			1.32	V
	Minimum negative overshoot	-0.1			V
AVDD12	Analog power supply	1.14	1.2	1.26	V
T	Operating temperature	-20		80	°C

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-41. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C

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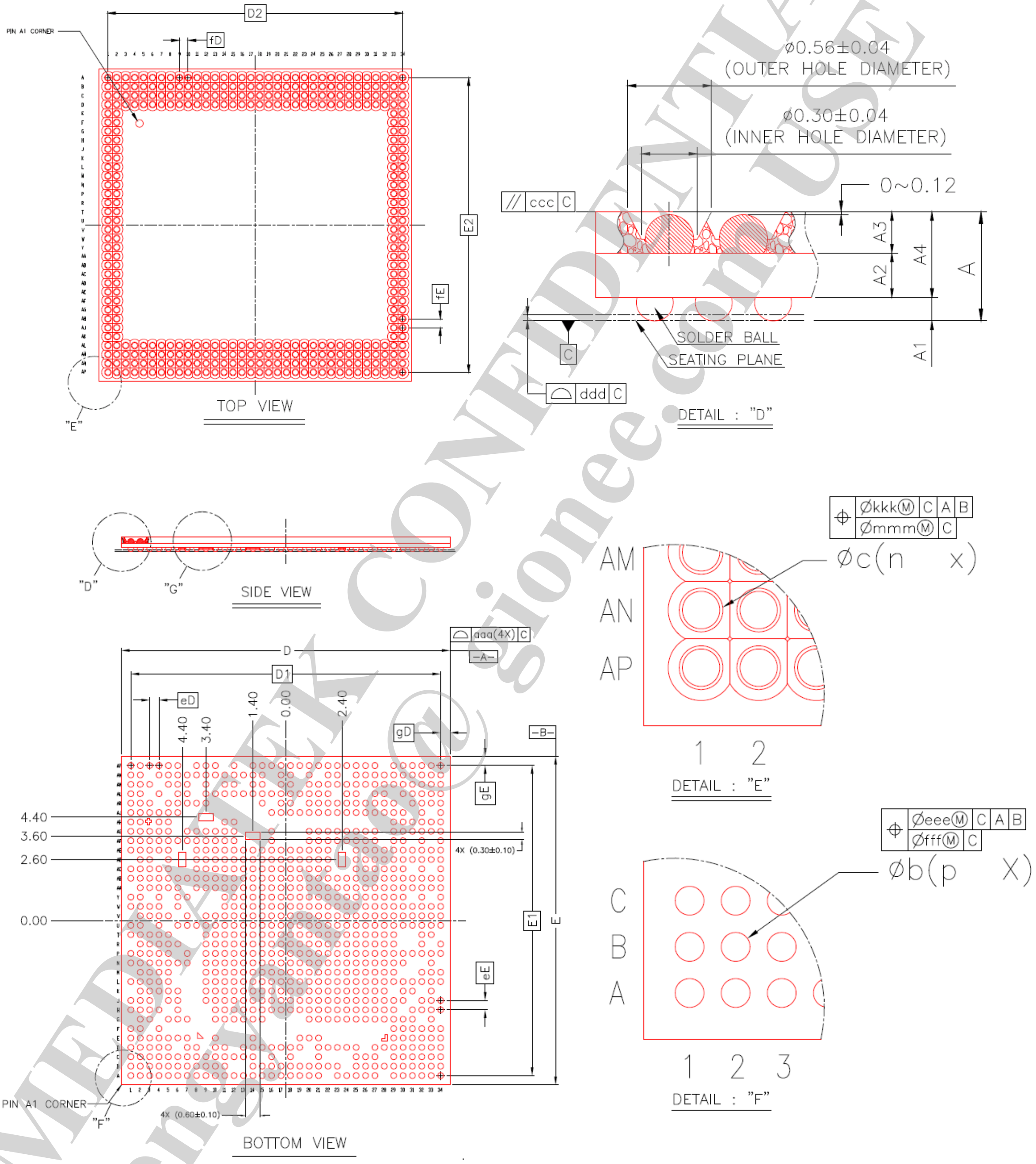
2.6 Package Information

2.6.1 Package Outlines



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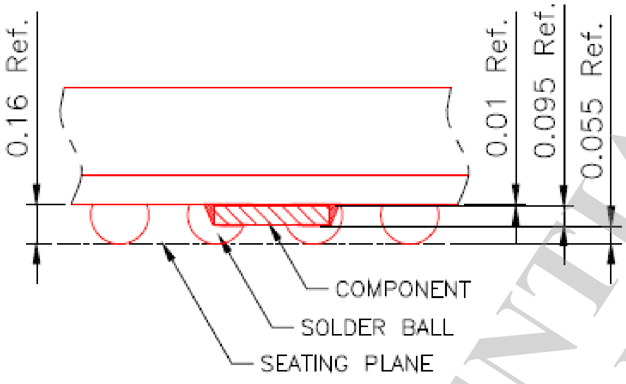

DETAIL : "G" : SYMBOL TYPE:0201

TOP SIDE INFORMATION					
Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Ball Pitch	X	fD		0.40	
	Y	fE		0.40	
Ball Diameter				0.25	
Ball Width		c	0.20	0.25	0.30
Ball Offset (Package)		kkk		0.15	
Ball Offset (Ball)		mmm		0.05	
Ball Count		n		376	
Edge Ball Center to Center	X	D2		13.20	
	Y	E2		13.20	

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BOTTOM SIDE INFORMATION					
Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MWFPOP		
Body Size	X	D	13.9	14.0	14.1
	Y	E	13.9	14.0	14.1
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.25 Ref.		
Substrate Thickness		A2	0.196 Ref.		
Substrate+Mold Thickness		A4	0.406	0.446	0.486
Total Thickness		A	–	–	0.666
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.10		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	930		
Edge Ball Center to Center	X	D1	13.20		
	Y	E1	13.20		
Edge Ball Center to Package Edge	X	gD	0.40		
	Y	gE	0.40		

Figure 2-37. Package outlines and dimensions

2.6.2 Thermal Operating Specifications

Table 2-42. Thermal operating specifications

Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	125	°C	
	Package thermal resistances in nature convection	21.28	°C/Watt	

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2.6.3 Lead-free Packaging

MT6799 is provided in a lead-free package and meets RoHS requirements.

2.6.4 MSL

MSL of this chip is 3.

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2.7 Power Delivery Network

Table 2-43. PDN specifications

Power rail	RDC (mohm)	Remote (mohm)	Frequency Range	Equivalent RLC Model
VPROC1	5.5	0.75	10K~100MHz	C=30.5uF, R=6mOhm , L=140pH
VPROC2	9	1		C=30.5uF, R=6mOhm , L=140pH
VGPU	5	0.5		C=35.5uF, R=8.5mOhm , L=80pH
VCORE	22	0.5		C=47.5uF, R=9.5mOhm , L=60pH
VCORE_C2K	45	22		C=47.5uF, R=37mOhm , L=0.95nH
VCORE_DDR_A (B, C, D)	35	15		C=47.5uF, R=30mOhm , L=0.6nH
VIMVO	80	5		C=28uF, R=35mOhm , L=0.55nH
VMD1	30	2		C=29uF, R=25mOhm , L=140pH
VMODEM	45	2		C=29u , R=25mOhm , L=140pH
VDD2_DRAM_A (B, C, D)	50	25		C=59.5uF, R=35mOhm , L=0.3nH
VDD2_A (B, C, D)	50	25		C=59.5uF, R=70mOhm , L=0.85nH
VDDQ_DRAM_A (B, C, D)	30	20		C=34.5uF, R=30mOhm , L=0.4nH
VDDQ_A (B, C, D)	30	20		C=34.5uF, R=30mOhm , L=0.8nH
VSRAM_PROC1	200	N/A		C=2uF, R=45mOhm , L=0.85nH
VSRAM_PROC2				
VSRAM_GPU1	100	N/A		C=2.2uF, R=80mOhm , L=0.5nH
VSRAM_GPU2				
VSRAM_CORE	150	N/A		C=2uF, R=45mOhm , L=0.65nH
VSRAM_MD	200	N/A		C=2uF, R=60mOhm , L=0.65nH

Note: Refer to document "MT6799_PDN_Checking_Notice.pdf" on DCC for more design concepts.

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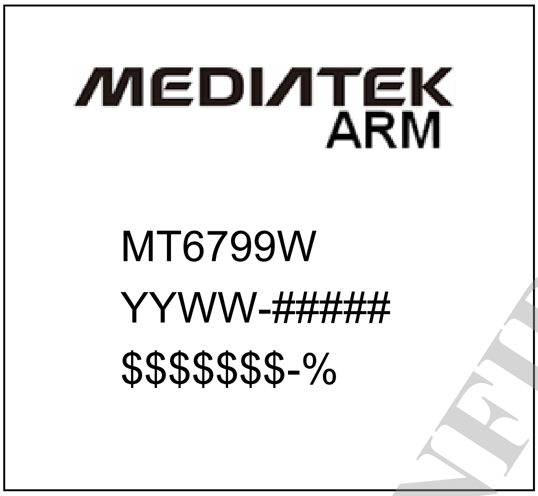
2.8 Ordering Information

2.8.1 Top Marking Definition



- YYWW: Date code
- #####: Subcontractor code
- $$$$$$$: LOT No.
- %: Application code

Figure 2-38. Top marking of MT6799

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